Journal of Advanced Research in Applied Sciences and Engineering Technology

Journal homepage:
https://semarakilmu.com.my/journals/index.php/applied_sciences_eng_tech/index
ISSN: 2462-1943

Design of 3.1-10.6 GHz UWB CMOS Power Amplifier using Cascade Topology

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ARTICLE INFO

Article history:
Received 3 May 2023
Received in revised form 28 August 2023
Accepted 7 September 2023
Available online 5 October 2023

Keywords:
CMOS; power amplifier; Ultra-wideband cascade topology

ABSTRACT

Power amplifier is an important component in the wireless communication system. Design of the power amplifier in UWB transceiver is challenging as the signal need to be transmitted over a wide bandwidth. Several criteria need to be fulfilled such as good linearity, good wideband matching, high efficiency and low power consumption. This paper presents the design of a power amplifier with 3.1-10.6 GHz using 0.18 µm CMOS technology for ultra-wide band application. The proposed power amplifier used three cascaded amplifier stages in order to achieve good gain and wide-band width. The results show that the proposed power amplifier design has an average gain of 7.28 dB, an input return loss less than -7.48 dB, an output return loss less than -4.782 dB, and group delay variation of ±151.9 ps is achieved over the entire band. A good input 1dB-compression point of 6.67 dBm and input third order intercept point of 0 dBm is achieved at 5 GHz.

1. Introduction

The rapid growth in modern technology, especially in wireless communication systems such as ultra-wideband (UWB), wireless personal area network (WPAN) and wireless local area network (WLAN) enabling users to communicate anywhere any time. This has become a necessity in our daily life. In February 2002, the Federal Communication Commission (FCC) has allowed the data transmission in the wide-ranging frequency of 3.1 to 10.6 GHz that allows data transmission at a higher rate of 100 to 500 Mbps with low power consumption [1]. As a result, the UWB has been considered as one of the most promising wireless technologies because of its ideal benefits such as low cost, high data rates, low power, low interference, and precise positioning.

Power amplifier is an important block in the wireless communication system. It is normally located at the final stage in the transmitter unit. It amplifies the signal and generates enough power

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https://doi.org/10.37934/araset.32.3.190198

to allow the signal to transmit over the required range. Power amplifier is one of the most challenging devices to design in UWB transceiver since it is required to transmit the signal over a wide bandwidth. It must meet several requirements such as good linearity, good wideband matching, high efficiency and low power consumption. Numerous UWB CMOS power amplifiers have been reported with frequency of 3.0–5.0 GHz, 3.0-7.0 GHz, 6.0–10.0 GHz and 3.1-10.6 GHz with various types of implemented topologies such as distributed amplifier, resistive shunt feedback and RLC matching, current-reused approach, common source inductive degeneration, current-reused technique, inter-stage wideband impedance transformer and stagger tuning [2-11]. Wideband matching in power amplifier design can be accomplished using distributed amplifiers, however, this topology consumes high power and large chip area [12]. Shunt-peaking technique is employed to provide wideband matching, but it affects the input and output matching. Resistive shunt feedback offers wideband matching and good input and output matching. This method results in a smaller chip area than other methods since it has less or no inductors. Inductive source degeneration has the potential to provide good input wideband matching as well as to enhance the linearity but lower the gain of the amplifier [9]. The advantage of using current-reused technique is to reduce power consumption, but it is quite difficult to meet the gain and wide frequency band from 3.1 to 10.6 [12]. In this paper, a design of 3-10.6 GHz UWB CMOS power amplifier by using cascade topology is proposed. The proposed UWB power amplifier implemented with 0.18 µm CMOS technology has obtained good parameters such as gain and linearity within the frequency of 3.1-10.6 GHz.

2. Methodology

The parameters for the proposed power amplifier design specifications are shown in Table 1 and the design is shown in Figure 1.

Table 1
Power amplifier design specification

Parameter	Specification
Frequency (GHz)	3.1-10.6
Gain (S_{21}) (dB)	>10
Input return loss (S_{11})	<-5
Output return loss (S_{11})	<-5
Reverse isolation, S_{12} (dB)	<-30
Input P1dB	>22
Output P1dB (dBm)	≈0
Group delay (ps)	<±100
Power consumption (mW)	<100

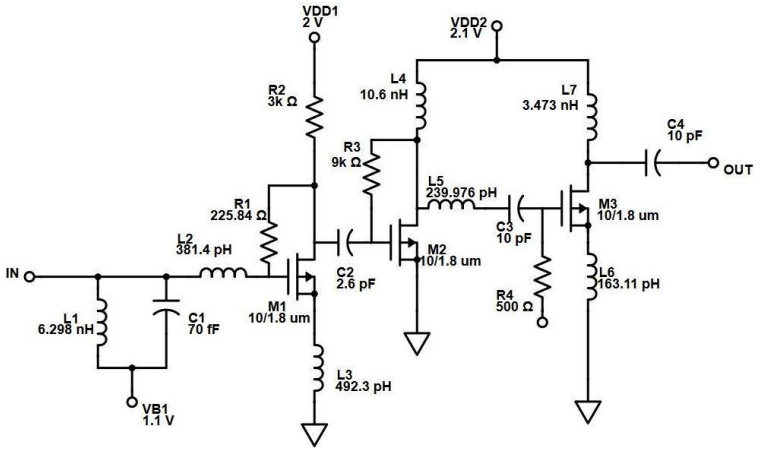

Fig. 1. Proposed UWB power amplifier design

The proposed UWB power amplifier design has three cascaded amplifier stages. The first stage, LC filter of C_1 and L_1 are used as the input matching network. Resistive shunt feedback of R_1 provides wider bandwidth and high value of inductive source degeneration, L_3 is used to improve the input matching. The inter-stage between the first and second stage consists of C_2 that performs as a coupling capacitor. The coupling capacitor in inter-stage is employed to block the DC current. The resistive shunt feedback of R_3 is used to improve the gain. The second stage is a simple common-source topology to maintain the high gain of S_{21} parameter. The next inter-stage between second and third stage consists of the LC filter, L_5 and C_3 to improve gain flatness. The third stage has source degeneration inductor, L_6 and the output matching involved single capacitor, C_4 to improve output matching. Each transistor in all stages (M_1, M_2, M_3) is set to 10/1.8 µm to stabilize the gain since the transistor is an active device that can affect the overall performance. Inductor L_3 is used as inductive source degeneration in the first stage of power amplifier to improve the linearity and stability of the amplifier. It is also utilized to improve the input wideband matching. The transmitter circuit is designed to have input impedance, Z_{in} of 50 Ω, centre frequency of 7 GHz, and transistor noise contribution, g_m of 40 mS. X_{C1} is a capacitive reactance for a capacitor, C_1. The calculation for inductor L_3 is shown in Eq. (1).

$$Z_{in} = jwL_3 + \frac{1}{jwC_{gs}} \tag{1}$$

whereas

$$w = 2\pi f_c \tag{2}$$

$$C_{gs} \approx \frac{g_m}{w_T} \tag{3}$$

3. Results

The proposed power amplifier design was implemented in 0.18 µm CMOS technology with 1.8 V supply voltage. A post layout of the proposed power amplifier is shown in Figure 2.

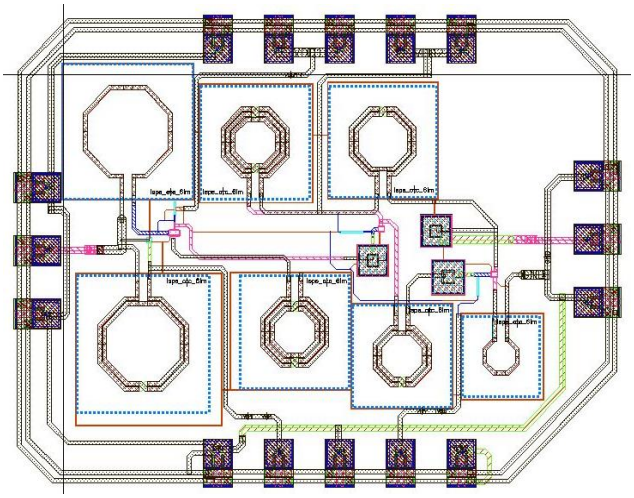

Fig. 2. Post layout of proposed UWB power amplifier design

The input return loss, S_{11} is shown in Figure 3. As can be seen from the post-layout result, the input return loss at 3.0 GHz is -7.48 dB and continuously decreases until -14.95 dB at 4.8 GHz and it increased up to -6.12 dB at 10 GHz. The post-layout result shows a better input matching graph compared to schematic result which is less than -5.13 dB. The difference between the schematic and post-layout is due to the parasitic circuit elements of capacitance and resistance that exist in post-layout design [13]. Parasitic elements are unavoidable in high frequency circuit design; however, it can be minimized by designing a layout as symmetrical as possible [14]. The minimum value of the input return loss in target property of UWB application is <-5 dB [15]. Since the simulation result shows the input return loss is less than -5 dB, the input matching of 50 Ω is achieved. The minimum points in the graph means that it has achieve highly accurate 50 Ω input matching [14].

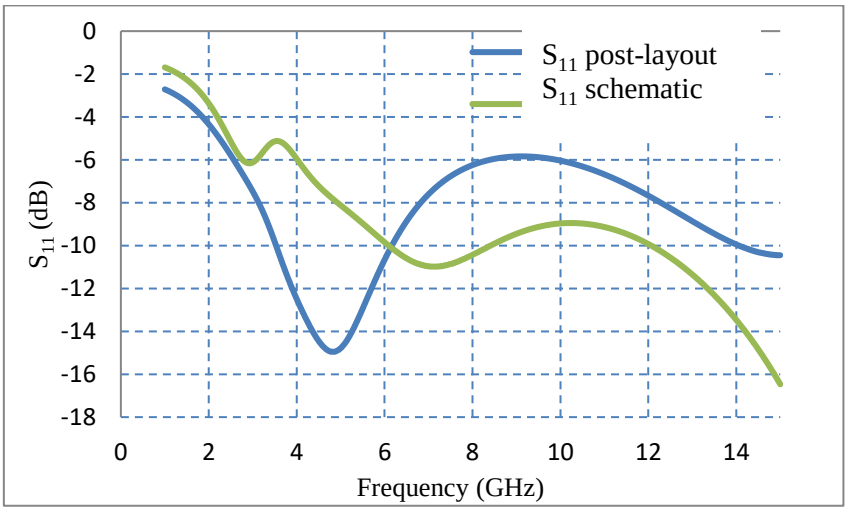

Fig. 3. Simulated S_{11} parameter

Simulated reverse isolation is illustrated in Figure 4. The result shows that the proposed UWB power amplifier has achieved good reverse isolation for both schematic and post-layout results of -35 dB over the frequency range of 3.0 to 10.6 GHz. This indicates that a high reverse isolation is achieved to prevent the leakage signal from transmitting to the antenna.

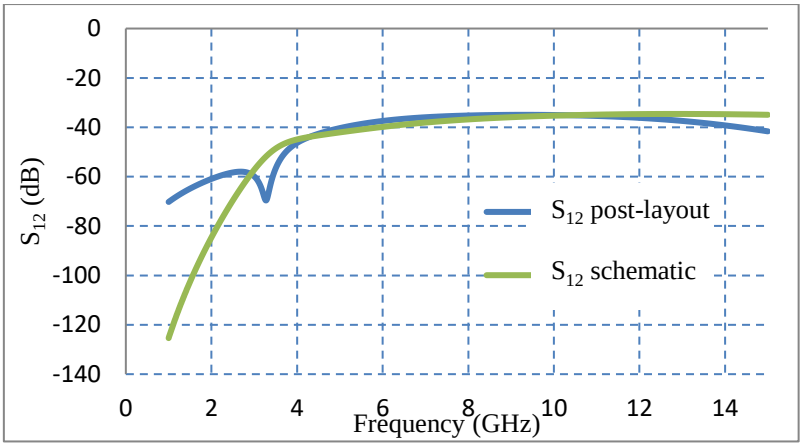

Fig. 4. Simulated S_{12} parameter

The average gain, S_{21} for post-layout and schematic of the proposed UWB power amplifier is shown in Figure 5. As can be seen, the S_{21} for post-layout and schematic are 7.28±5.73 dB and 15.92±4.70 dB, respectively. The average gain for post-layout decreases almost half of the schematic gain due to the parasitic element effects. The gain flatness for both post-layout and schematic results were quite poor due to the high value of R_3 which is 9 kΩ. However, if we reduce the value of R_3, it would decrease the gain obtained since it is used to support the second stage.

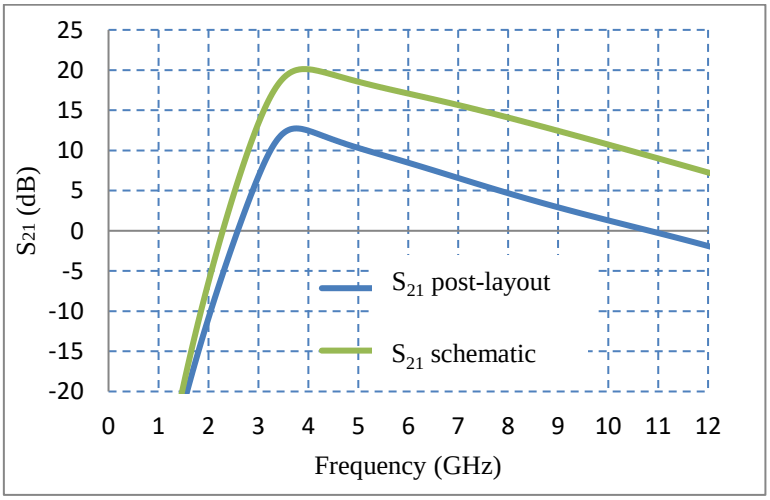

Fig. 5. Simulated S_{21} parameter

The output return loss, S_{22} for proposed UWB power amplifier is depicted in Figure 6. The output return loss obtained are -3.141 dB for schematic and -4.782 dB for post-layout. As can be seen, the output return loss for post-layout at 3.0 GHz is -4.782 dB and continuously decreasing until -23.97 dB at 4.0 GHz and it increases up to -4.6 dB at 10 GHz. Minimum acceptance of output return loss is less than -5 dB [14]. This means that our proposed design has good return loss and achieved 50 Ω output matching. The smaller value of S_{22} indicates a better output matching of the power amplifier. Hence, the narrow shape at the minimum points of <-23.97 dB and <-27.45 dB in the graph shows that the circuit has a very good output matching to 50 Ω load. This enables the optimum delivery of power levels by knowing what load and source impedance are seen by the Device Under Test (DUT) [15].

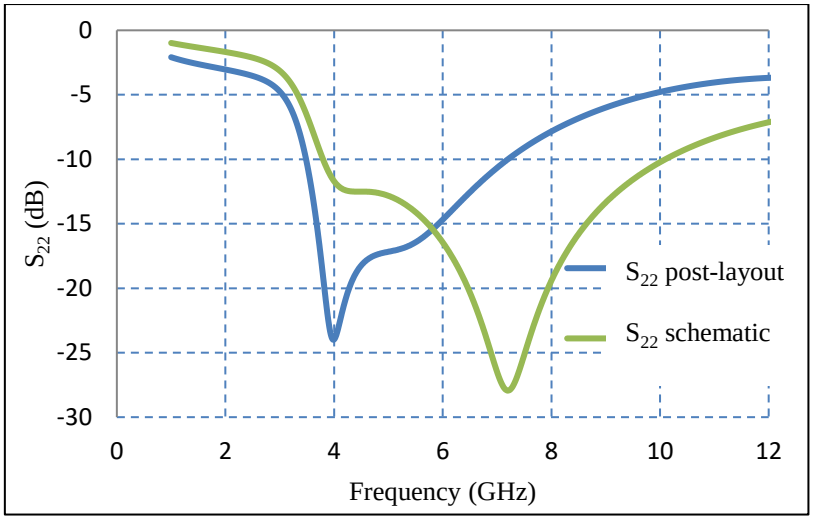

Fig. 6. Simulated S_{22} parameter

Figure 7 shows the stability simulation result that has been computed through the S-parameter analysis. It clearly shows that the proposed UWB power amplifier is unconditionally stable as the stability factor of more than 10.6 is obtained over the entire band.

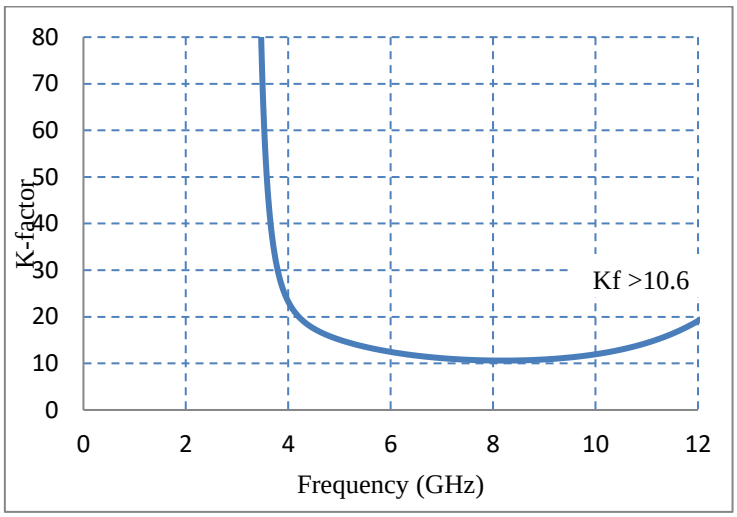

Fig. 7. K-factor

The group delay variation is illustrated in Figure 8. This parameter is very important since it indicates that the output signal will not be distorted and can retain its original identity through the power amplifier. The proposed UWB power amplifier design has obtained group delay variation of ±151.9 ps over frequency range of 3.0 to 10.6 GHz.

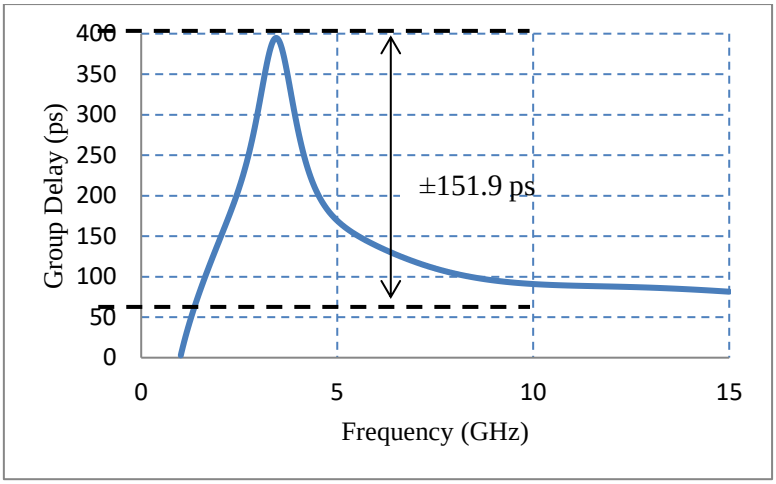

Fig. 8. Group delay variation

Figure 9 shows that the output referred 1-dB compression point is 6.67 dBm at the input referred 1-dB compression point of -10 dBm at centre frequency of 5 GHz. The 1-dB compression point indicates where the input and output level of the gain has dropped by 1 dB.

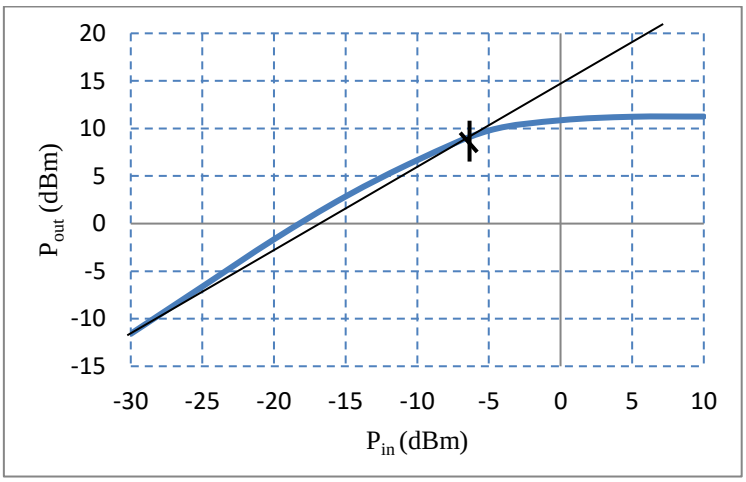

Fig. 9. 1-dB compression point

The third-order intercept point (IP3) is obtained from the plotted output power (P_{out}) versus input power (P_{in}) as shown in Figure 10. This point indicates the power level of the distortion signal begin to overtake the fundamental signal. The input referred IP3 and output referred IP3 are -9 dBm and 9.8 dBm, respectively. These results show that the UWB power amplifier have good linearity since it is near to 0 dBm.

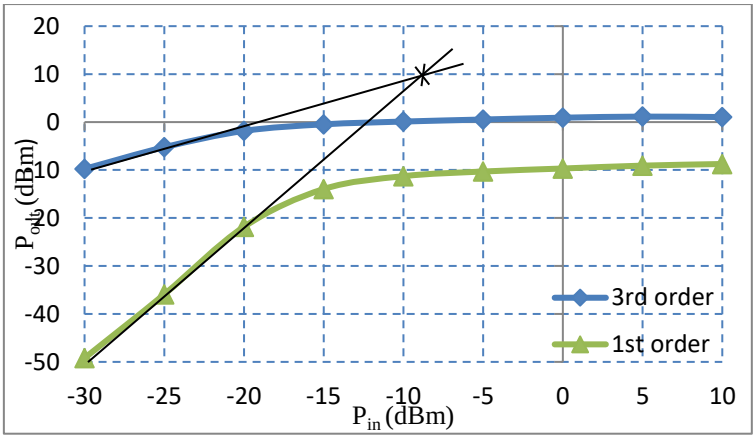

Fig. 10. Third-order intercept point

4. Conclusions

A full band of 3.0-10.6 GHz power amplifier for UWB application was successfully designed using Silterra 0.18 µm CMOS technology. The proposed power amplifier used three cascade amplifier stages to achieve good gain over 3.0 to 10.6 GHz frequency. However, the input and output matching are not adequate enough, this can be improved by implementing external input and output matching circuit in the design. For future research, it is interesting to investigate and design the topology that can reduce power consumption and low group delay variation.

Acknowledgement

The author would like to thank Ministry of Higher Education, Malaysia, Fundamental Research Grant Scheme (FRGS/1/2020/TK0/UNIMAS/02/6) and Universiti Malaysia Sarawak (F02/FRGS/2005/2020) for supporting this work.

References

[1] Sweet, Allen A. *Designing bipolar transistor radio frequency integrated circuits*. Artech House, 2007.

[2] Wong, Sew-Kin, Siti Maisurah, Mohd Nizam Osman, Fabian Kung, and Jin-Hui See. "High efficiency CMOS power amplifier for 3 to 5 GHz ultra-wideband (UWB) application." *IEEE Transactions on Consumer Electronics* 55, no. 3 (2009): 1546-1550. https://doi.org/10.1109/TCE.2009.5278025

[3] Sapawi, R., A. N. Asyraf, D. H. A. Mohamad, S. K. Sahari, S. M. W. Masra, K. Kipli, N. Julai, N. Junaidi, D. N. S. D. A. Salleh, and S. A. Z. Murad. "High gain of 3.1-5.1 GHz CMOS power amplifier for Direct sequence ultra-wideband application." *Journal of Telecommunication, Electronic and Computer Engineering (JTEC)* 8, no. 12 (2016): 99-103.

[4] Murad, S. A. Z., R. K. Pokharel, A. I. A. Galal, R. Sapawi, H. Kanaya, and K. Yoshida. "An excellent gain flatness 3.0-7.0 GHz CMOS PA for UWB applications." *IEEE Microwave and Wireless Components Letters* 20, no. 9 (2010): 510-512. https://doi.org/10.1109/LMWC.2010.2052593

[5] Chung, H-W., C-Y. Hsu, C-Y. Yang, K-F. Wei, and H-R. Chuang. "A 6-10-GHz CMOS power amplifier with an inter-stage wideband impedance transformer for UWB transmitters." In *2008 38th European Microwave Conference*, 305-308. IEEE, 2008. https://doi.org/10.1109/EUMC.2008.4751449

[6] Lu, Chao, A-V. Pham, and Michael Shaw. "A CMOS power amplifier for full-band UWB transmitters." In *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, 2006, 4-pp. IEEE, 2006.

[7] Ali, Mayar, Hesham FA Hamed, and Ghazal A. Fahmy. "Small group delay variation and high efficiency 3.1-10.6 GHz CMOS power amplifier for UWB systems." *Electronics* 11, no. 3 (2022): 328. https://doi.org/10.3390/electronics11030328

[8] Mosalam, Hamed, Ahmed Allam, Hongting Jia, Adel B. Abdel-Rahman, and Ramesh K. Pokharel. "High Efficiency and Small Group Delay Variations 0.18- µm CMOS UWB Power Amplifier." *IEEE Transactions on Circuits and Systems II: Express Briefs* 66, no. 4 (2018): 592-596. https://doi.org/10.1109/TCSII.2018.2870165

[9] Sapawi, R., D. H. A. Mohamad, D. S. A. A. Yusuf, S. K. Sahari, D. N. S. D. A. Salleh, N. A. H. A. Hazis, and S. A. Z. Murad. "CMOS Power Amplifier Design Techniques for UWB Communication: A Review." *Journal of Telecommunication, Electronic and Computer Engineering (JTEC)* 9, no. 2-10 (2017): 1-8.

[10] El-Feky, Nagham G., Dina M. Ellaithy, and Mostafa Fedawy. "3-5 GHz CMOS power amplifier in 130nm CMOS for UWB applications." In *2022 9th International Conference on Electrical and Electronics Engineering (ICEEE)*, pp. 32-35. IEEE, 2022. https://doi.org/10.1109/ICEEE55327.2022.9772578

[11] Jose, Sajay. "Design of RF CMOS Power Amplifier for UWB Applications." *PhD diss., Virginia Tech*, 2004.

[12] Grewing, Christian, Kay Winterberg, Stefan van Waasen, Martin Friedrich, Giuseppe Li Puma, Andreas Wiesbauer, and Christoph Sandner. "Fully integrated distributed power amplifier in CMOS technology, optimized for UWB transmitters." In *2004 IEE Radio Frequency Integrated Circuits (RFIC) Systems*. Digest of Papers, 87-90. IEEE, 2004.

[13] Wolf, Wayne. *Modern VLSI design: system-on-chip design*. Pearson Education, 2002.

[14] Sapawi, Rohana, Ramesh K. Pokharel, Haruichi Kanaya, and Keiji Yoshida. "A wide range CMOS power amplifier with improved group delay variation and gain flatness for UWB transmitters." *IEICE Transactions on Electronics* 95, no. 7 (2012): 1182-1188. https://doi.org/10.1587/transele.E95.C.1182

[15] Mat, D. Azra Awang, N. Syuhada Hasim, Nurmiza Othman, Amira Amran, D. Norkhairunnisa Abang Zaidel, AS Wani Marzuki, Shafrida Sahrani, and Rohana Sapawi. "Integrated open loop resonator filter designed with notch patch antenna for microwave applications." *TELKOMNIKA (Telecommunication Computing Electronics and Control)* 15, no. 3 (2017): 1485-1492. https://doi.org/10.12928/telkomnika.v15i3.7218