SEMARAK ILMU PUBLISHING

Journal of Advanced Research in Applied Mechanics

Journal homepage:
https://semarakilmu.com.my/journals/index.php/appl_mech/index
ISSN: 2289-7895

Development of Converter for Linear Wave Energy Stabilizer by Replacing the Inductor Type from the Existing Modified SEPIC Circuit

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ARTICLE INFO

Article history:
Received 28 June 2023
Received in revised form 30 August 2023
Accepted 15 September 2023
Available online 24 October 2023

Keywords:
SEPIC; modified SEPIC; MATLAB Simulink

ABSTRACT

Wave is one of the renewable resources that can replace non-renewable resources to reduce the Green House Gas (GHG) emission. Other than wave geographical location and condition, the electronics technical design and components used also plays an important role to maximize the capture of wave energy. DC-DC converter topologies have been widely used in power conversions. However, wave energy has no uniform pattern making the electricity energy generated by it is unclean. Furthermore, there is no small-scale converter specifically for pico-scale linear generator which require high static gain to capture wave energy. With the aim to improve the performance of energy conversion, this paper proposed a new converter design based on the existing topology which is modified SEPIC. The simulation for the two converters is performed to identify the percentage of performance improvement by using MATLAB Simulink software before fabricating a prototype. The comparison of experimental and simulation data for the converters is conducted and analysed in this paper to validate its percentage of error. From the results obtained, it is proven that the modification made from the existing topology improved significantly to the overall performance of the converter.

1. Introduction

The consumption of electricity keeps on increasing gradually as technology progresses and the main energy resources for electricity generation which are from non-renewables family such as earth minerals, metal ores and fossil fuel are hazardous to the surrounding and degrade the quality of air. They are expected to be entirely depleted years from now as discussed in energy article webpage [1]. From the information taken from the report of Intergovernmental Panel on Climate Change [2], wave energy has the potential to generate around 32,000Twh of electricity. From the previous study [3], Existing WEC (Wave Energy Converter) designs can only harness huge amounts of wave energy to convert to electricity and due to that limitation, many researchers have started to do innovations to encounter such issues. Waves energy generated by sea is not uniform and when converted to electrical energy, it is also in non-uniform state. In order to stabilize the converted signal, it is required

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https://doi.org/10.37934/aram.110.1.97111

for the signal to be changed to DC form. There are types of rectifiers to do the tasks such as center tapped and full-wave bridge rectifier. However, the analysis conducted in [4, 5] shows center tapped rectifier has advantages like high peak reverse voltage, Vrrm and high VA rating. But, if considering the physical size, cost, and circuit simplicity, full-wave bridge rectifier is most suitable to conduct such task. The converted DC signal consists of AC components and it has to be filtered out. Filter circuit is required to clean the noisy electrical signal. There are filter circuits that can perform the task, for example LC filter, Choke Input L-Section filter, Capacitance Input filter, RC filter and so forth. From the analysis and research conducted in [6, 7], RC filter, which consists only a capacitor and a resistor to form a low-pass filter, is among all has the least drawbacks and can combat the problems faced by other filter types, it is also the simplest filter design and suitable for common signal filtration purpose. DC-DC converters topologies such as buck, boost, buck-boost, Cuk, SEPIC, and modified SEPIC have been widely used in many applications for power conversion, DC motor drive application, regulated switched mode DC power supply and many more. The previous study [8] shows that the most common application of DC converter is in UPS (Uninterruptable Power Supply) system where the output needs to be varied and regulated throughout the operation time. The input to these DC converters is often unregulated. The unregulated DC input voltage can be converted into controlled DC output at a desired voltage level by using switch mode DC-DC converters. At present, the demand for high efficiency of step-up DC-DC converters is increasing steeply specifically for battery powered equipment with less power storage. The past research [9] finds that there are applications required to have high step-up static gain and high efficiency for instance, adjustable speed drive, battery charging for electric vehicles, telecommunication system power supply, battery storage systems, and so forth. Furthermore, the crucial part when designing high efficiency converters is at the step-up stage where the input current and output voltage both need to be high. The typical boost converter topology can regulate the output voltage. However, the previous analysis conducted in previous research [10] shows that the boost converter has high switching loss when the AC line voltage is low where the input current is high and demands high step-up conversion. For the converter to work with low AC line voltage and high input current, the inductor must be robust and have a high inductance rating. Due to that, the boost converter is not suitable for low line voltage application. The study [11] finds that by Integrating voltage multiplier with classical DC converter introduces new operation features which makes it has high static gain suitable for step-up converter applications. There are many topologies that aim to improve the efficiency of DC converters as presented in past research [12-14]. However, the designs are complex, suitable for complex applications, higher components count and required addition control circuit to put them into operation. From literature survey conducted, there are no specific converter designs for pico-scale linear wave generator which has less complexity and less components count. In this paper, the new converter is designed based on the existing converter topology which is modified SEPIC (Single-Ended Primary Inductor Converter). The design is made in a way that it is not complex, less components counts, improves overall performance, and suits to be used with pico-scale linear wave generator.

2. Methodology

2.1 Circuit Operation

The configuration of the new proposed design is based on modified SEPIC circuit as illustrated in Figure 1 with the two uncoupled inductors are replaced with a coupled inductor and a diode is introduced and placed at the secondary side of the coupled inductor.

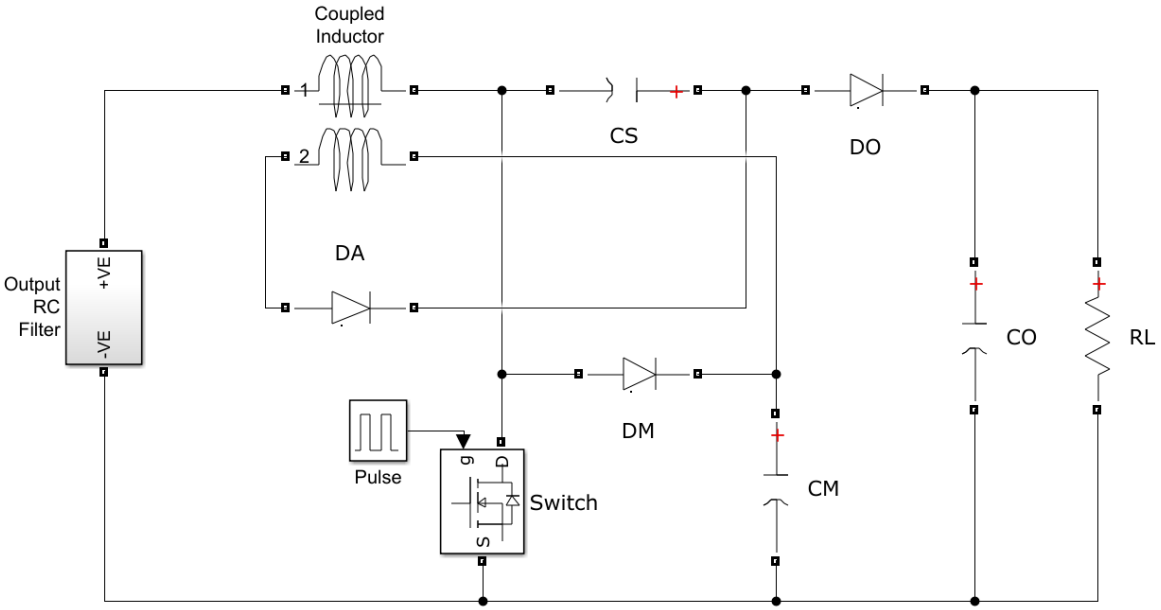

Fig. 1. Proposed Design Circuit

The operation of the proposed design is almost the same as modified SEPIC circuit. By assuming the circuit shown in Figure 2 (a) and (b) is in CCM (Continuous Conduction Mode), when the switch S is turned OFF, the primary side of the coupled inductor supplies the load RL through the capacitor CS and diode DO. The capacitor CM is being charged through diode DM. At this instant, the secondary part of the coupled inductor is supplying the load RL while increasing its energy from cutting the flux generated by the primary part of the coupled inductor. The diode DA is added between the capacitor CS and the secondary side of the coupled inductor. This is to block reverse current of the secondary part of the coupled inductor when it has completely discharged its energy when the switch S is turned OFF. Diode DA reduced current stress of secondary side of the coupled inductor since reverse current is inhibited.

When the switch S is turned ON, the diodes DM and DO are blocked because the current flows in reversed. At this cycle, both sides of coupled inductor are being charged up and increase their energy. On the secondary side, the energy is being generated by cutting the flux produced by the primary side. The primary side is charged by the main input voltage, VI while the voltage across CS and CM is applied to the secondary side. The voltage across capacitor CM is greater than the voltage across the capacitor CS. The advantages of the proposed circuit design are the settling time is shorter, the current flow through coupled inductor is improved significantly by inhibiting reverse current on the secondary side of coupled inductor, output voltage amplitude is slightly higher, less output voltage ripple, and current is always in CCM. Simulation results are presented in the result section.

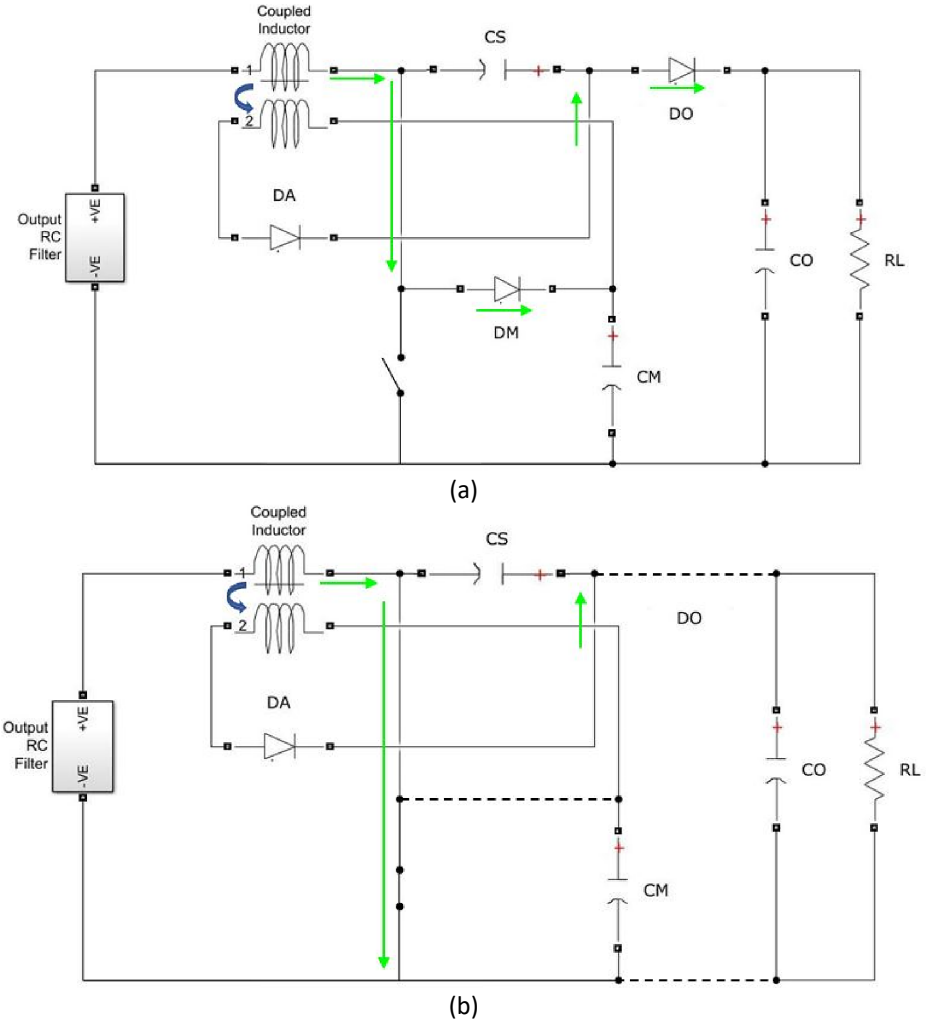

Fig. 2. Operation of Proposed Converter Design where (a) Off-state and (b) On-state

2.2 Comparison, Analysis and Design of the Circuit

The analysis and formulas for modified SEPIC are derived from the past study [15]. Static gain is defined as the ratio of the output to the input of the system design. It is the ability of the system to increase the power of the output from the input. When L1 is in steady state mode, the relation is as shown in Eq. (1) and Eq. (2).

$$V_i(t_{on} + t_{off}) = V_{CM} \times t_{off} \tag{1}$$

$$V_i D = (V_{CM} - V_i) \times (1 - D) \tag{2}$$

The same equation of the classical boost converter static gain is used to define voltage capacitor CM as defined by Eq. (3).

$$\frac{V_{CM}}{V_i} = \frac{1}{1-D} \tag{3}$$

During the conduction state of D0 and DM, the switch S is turned OFF (t_{off}) and the relation can be defined as shown in Eq. (4) and Eq. (5) below:

$$V_o = V_{cs} + V_{cm} \tag{4}$$

$$V_{cs} = V_o - V_{cm} \tag{5}$$

The relations shown in Eq. (6) and Eq. (7) can be considered during the steady state of L_2 since its average voltage is zero.

$$(V_{cm} - V_{CS}) \times t_{on} = (V_0 - V_{CM}) \times t_{off} \tag{6}$$

$$(V_{cm} - V_{CS}) \times D = (V_0 - V_{CM}) \times (1 - D) \tag{7}$$

The proposed converter static gain is obtained from the Eq. (3), Eq. (5) and Eq. (6) and it is presented in (8).

$$\frac{V_0}{V_i} = \frac{1+D}{1-D} \tag{8}$$

By substituting Eq. (3) and Eq. (8) into Eq. (7), the equation to define voltage of the capacitor CS is presented in Eq. (9).

$$\frac{V_{CS}}{V_i} = \frac{D}{1-D} \tag{9}$$

The classical SEPIC circuit static gain is similar as the Eq. (9) since the output voltage is the same as the voltage across capacitor CS. Therefore, the static gain of the classical SEPIC circuit is as shown in Eq. (10). The circuit operation with higher static gain gives significant improvement when operating with lower input voltage.

$$\frac{V_0}{V_i} = \frac{D}{1-D} \tag{10}$$

The equation to determine input current ripple (Δi_{L1}) is the same as the boost, classical SEPIC and modified SEPIC circuits as they are having the same input stage. When the switch is ON, Δi_{L1} is define by the Eq. (11).

$$\Delta i_{L1} = \frac{V_i \times D}{f_s \times L_1} \tag{11}$$

fs = Line Frequency

Since L1 is equal to L2, the value of inductance is calculated by using the Eq. (12) below:

$$L = L_1 = L_2 = \frac{V_i \times D}{f_s \times \Delta i_{L1}} \tag{12}$$

It is to be noted that the duty cycle obtained in Table 1 is by using the Eq. (8).

Table 1
Simulation and Experimental Data for the Proposed Stabilizer Circuit

Model Parameters	Values
Input Voltage, Vi	5V
Output Voltage, Vo	18V
Duty Cycle, D	57%
Switching Frequency, *fs*	50kHz
Supply Frequency, *f*	50Hz
Max Output Power, Po	2.036W
Max Input Current Ripple	18%
Capacitor Voltage Ripple	7%
Output Voltage Ripple	1%
Max Inductor L1 Current/ IRMS	1.017A
Max Inductor L2 Current	0.111A

The input current ripple can be calculated by using the Eq. (13) by plugging in the data of IRMS.chosen in Table 1.

Δi_{L1} = $\sqrt{2}$ × IRMS × 18% (13)

Δi_{L1} = $\sqrt{2}$ × 1.017A × 0.18 = **0.259A**

Substitute the value obtained from Eq. (13) into Eq. (12) to obtain the inductance value of L1 & L2.

$L = L1 = L2 = \frac{18V \times 0.57}{50kHz \times 0.259A}$ = **220µH**

During the switch S is turned ON, the current of inductor L2 is equal to the current in CS and CM capacitances. The charge variation of capacitor, ΔQ can be calculated by using the Eq. (14).

$\Delta Q = i_{L2} \times D \times T$ (14)

The Eq. (15) defines the high-frequency voltage attenuation, ΔV_C as a function of the capacitor charge variation.

$\Delta V_C = \frac{\Delta i_{L2} \times D \times T}{C}$ (15)

ΔV_C can also be calculated by using Eq. (16).

$\Delta V_C = 7\% \times V_o$ (16)

$\Delta V_C = 7\% \times 18V$ = **1.26V**

By equating the value obtained in the Eq. (16) the data in Table 1 into Eq. (17), the capacitance value of CS and CM are obtained.

$$C = C_M = C_S = \frac{i_{L2} \times D}{f_s \times \Delta V_C} \quad (17)$$

$$C = \frac{0.111A \times 0.57}{50kHz \times 1.26V} = \mathbf{1\mu F}$$

The capacitance value of CO is calculated by using the Eq. (18). The capacitance value is obtained by using the data provided in Table 1.

$$C_O = \frac{P_O}{2 \times \pi \times f \times 2V_O \times \Delta V_O} \quad (18)$$

$$C_O = \frac{2.036W}{2\times\pi \times 50Hz \times 2(18V) \times (0.18)} = \mathbf{1000\mu F.}$$

3. Results

The simulation comparison between the existing topology, Modified SEPIC and the proposed design converter is made. Figure 3 shows the circuit of the existing converter of Modified SEPIC circuit and Figure 4 shows the proposed design converter circuit.

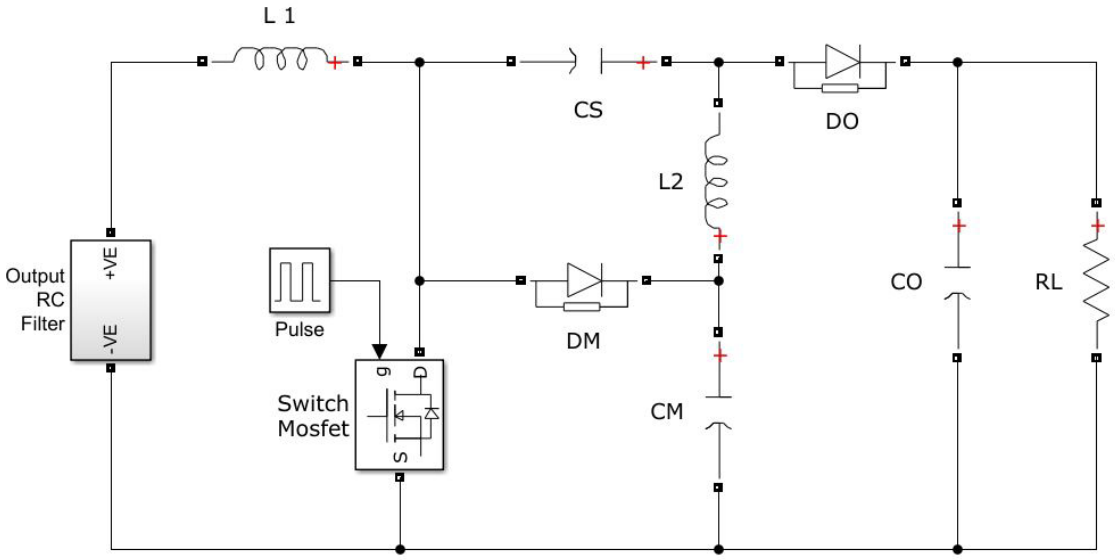

Fig. 3. Modified SEPIC Circuit

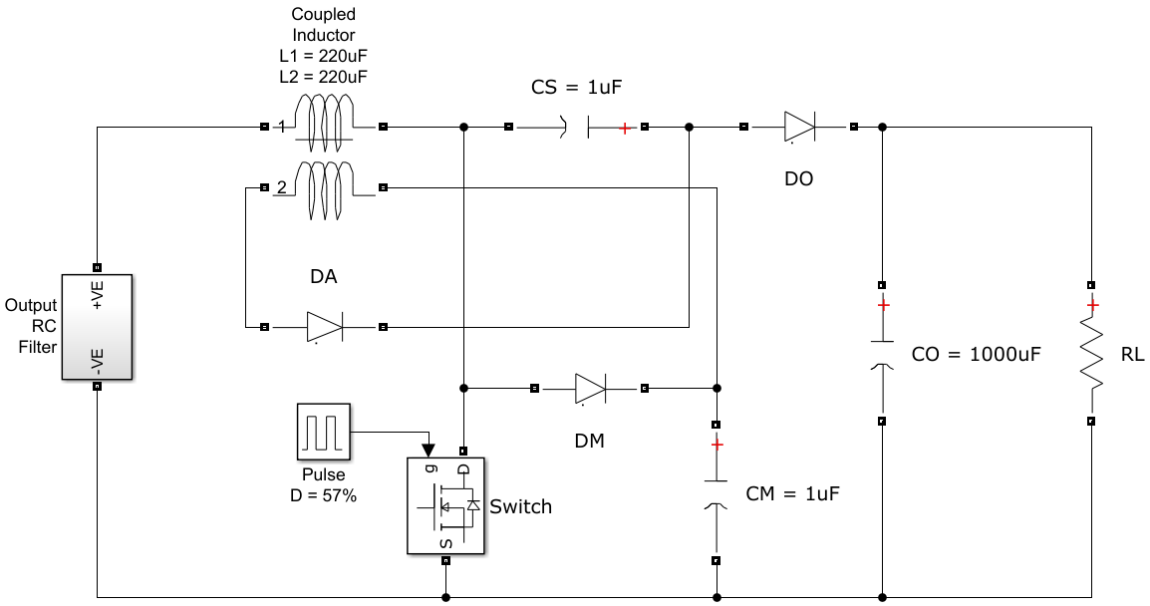

Fig. 4. Proposed Stabilizer Circuit

The simulation results of the two converters are analysed in terms of currents ripple, currents stability, output voltage amplitude and output voltage ripple. Figure 5 and Figure 6 show the currents stability of the converters.

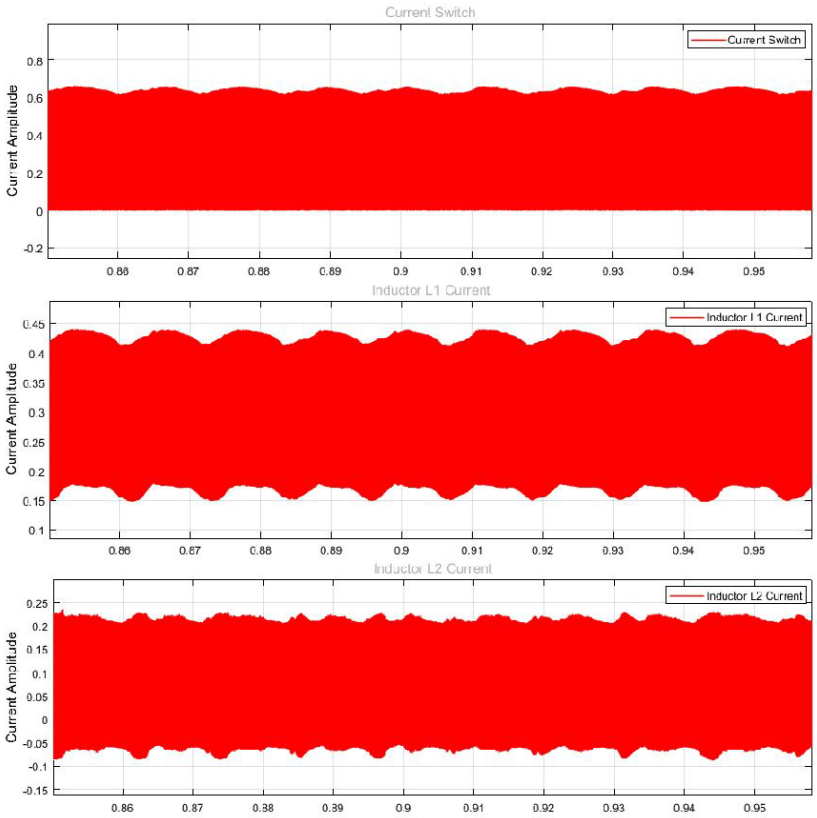

Fig. 5. Current Graphs of Modified SEPIC

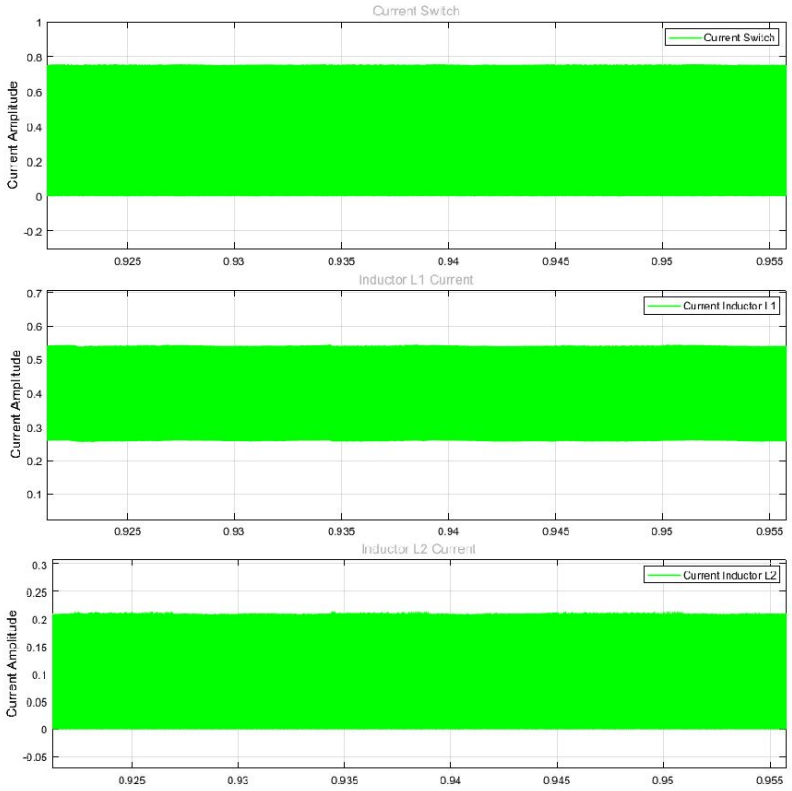

Fig. 6. Current Graphs of Proposed Design Converter

As per observation from the graph results obtained, all the currents of the proposed design converter have higher stability when compared to the existing Modified SEPIC circuit. This is due to the coupled inductor as every state of the converter (Switch ON & OFF) is energizing both sides of the coupled inductor. Figure 7 and Figure 8 show the zoomed-in of current graphs for both converters to analyse all the current ripples. The current switch of the proposed converter has higher amplitude when compared to the existing circuit. The inductor L1 current is having almost the same amplitude value for both converters. But the inductor L2 current of the proposed converter capped off when it reaches zero while the existing Modified SEPIC circuit continues until the current reverses. This is due to the diode DA installed after the secondary side of the coupled inductor on the proposed converter which it prohibits the reverse. All the current values are tabulated in Table 2 below.

Table 2
Currents Value for Both Converters

Modified SEPIC	Proposed Design Circuit
Current Switch = 0.6304A	Current Switch = 0.7476A
Inductor L1 Current = 0.2571A	Inductor L1 Current = 0.2780A
Inductor L2 Current = 0.2643	Inductor L2 Current = 0.2096A

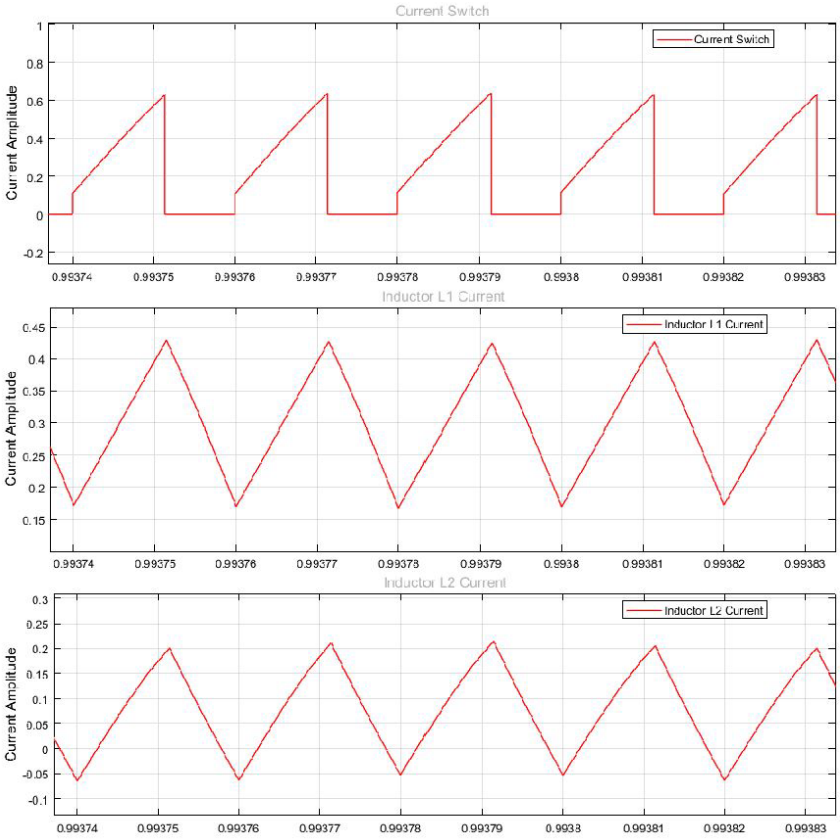

Fig. 7. Current Ripples of Modified SEPIC

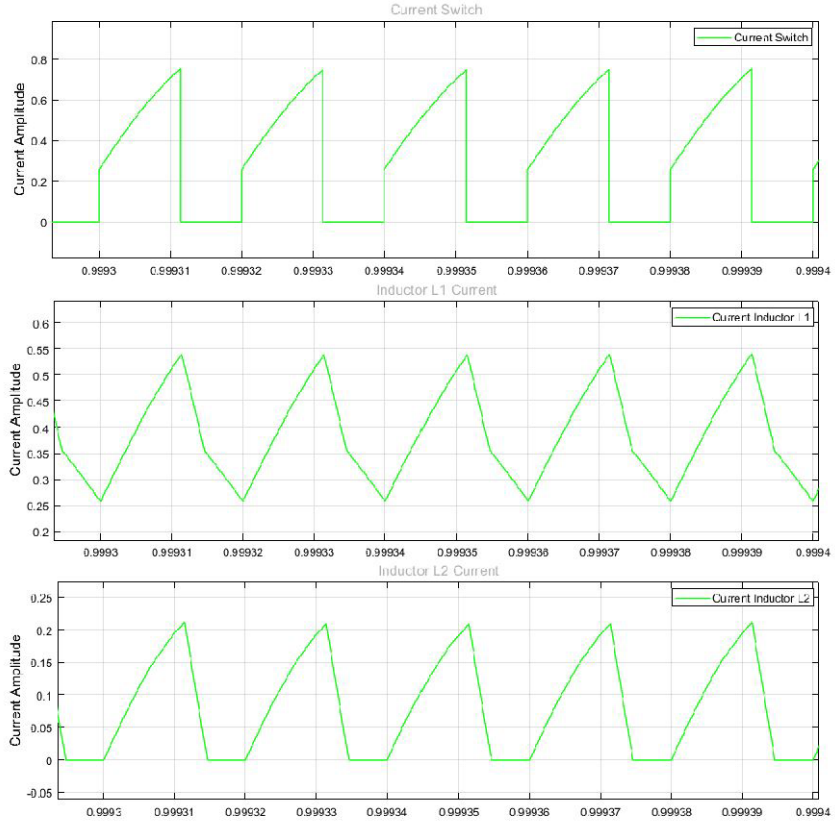

Fig. 8. Current Ripples of Proposed Design Converter

The comparison graph of the output voltage converter is as shown in Figure 9. The proposed design converter increases 9.42% of the output voltage amplitude when compared to the Modified SEPIC circuit. This shows there is a significant improvement of the static gain value. The graphs of output voltage ripples for the two converters are shown in Figure 10 and Figure 11. The ripple of output voltage for the proposed converter is less than the Modified SEPIC. All the values are tabulated in Table 3 below.

Table 3
Voltage Values for Both Converters

Modified SEPIC	Proposed Design Circuit
Output Voltage Amplitude = 16.88V	Output Voltage Amplitude = 18.47V
Voltage Ripple Amplitude = 0.01581V	Voltage Ripple Amplitude = 0.0009706V
Ripple Percentage = 0.094%	Ripple Percentage = 0.005%
Static Gain = 3.376	Static Gain = 3.694

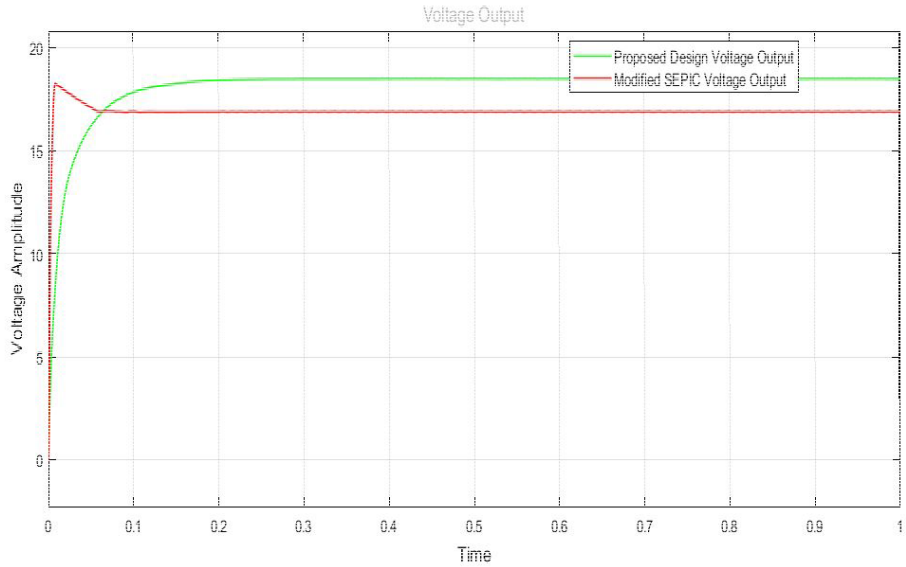

Fig. 9. Output Voltage of Proposed Converter vs Modified SEPIC Circuit

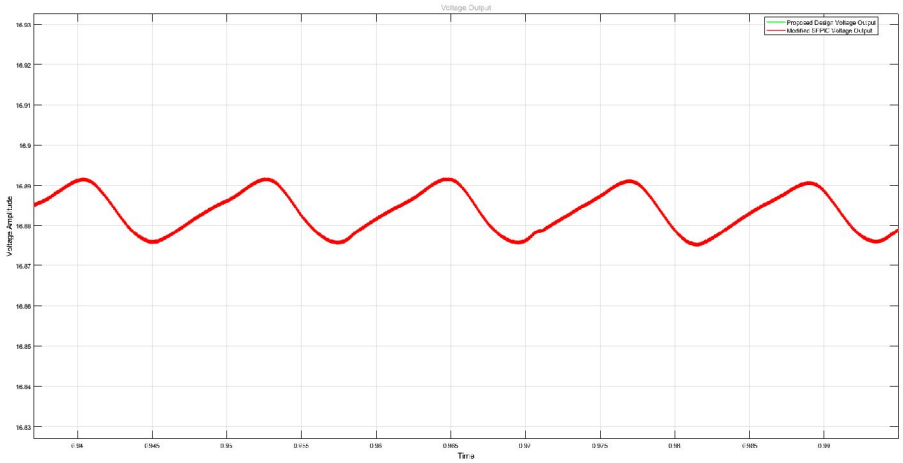

Fig. 10. Output Voltage Ripple of Modified SEPIC Circuit

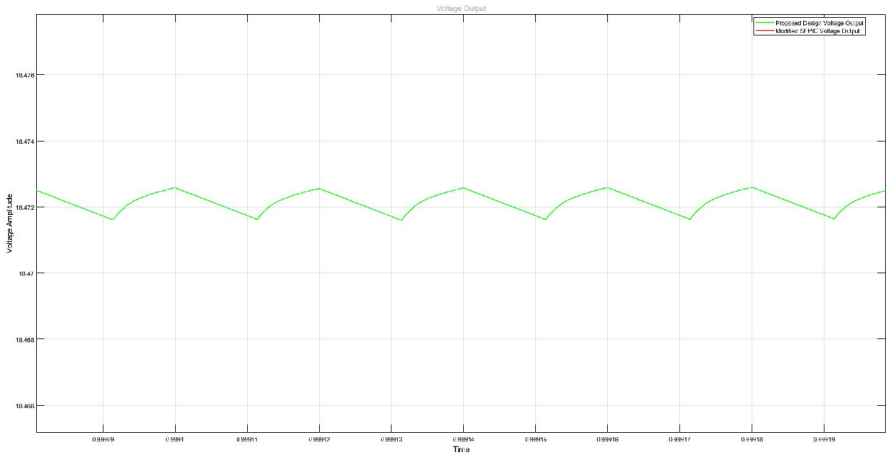

Fig. 11. Output Voltage Ripple of Proposed Design Converter

As per calculation made previously for the component's sizes and ratings for simulation and experimental analysis, all the values are presented in Table 4. Figure 12 shows the prototype of the proposed converter that is built and used to analyse the circuit experimentally.

Table 4
Components Sizes & Ratings

Components	Values
Inductor L1	220µH
Inductor L2	220µH
Mutual Inductance LM	220µH
Capacitor CS	1µF
Capacitor CM	1µF
Capacitor CO	1000µF

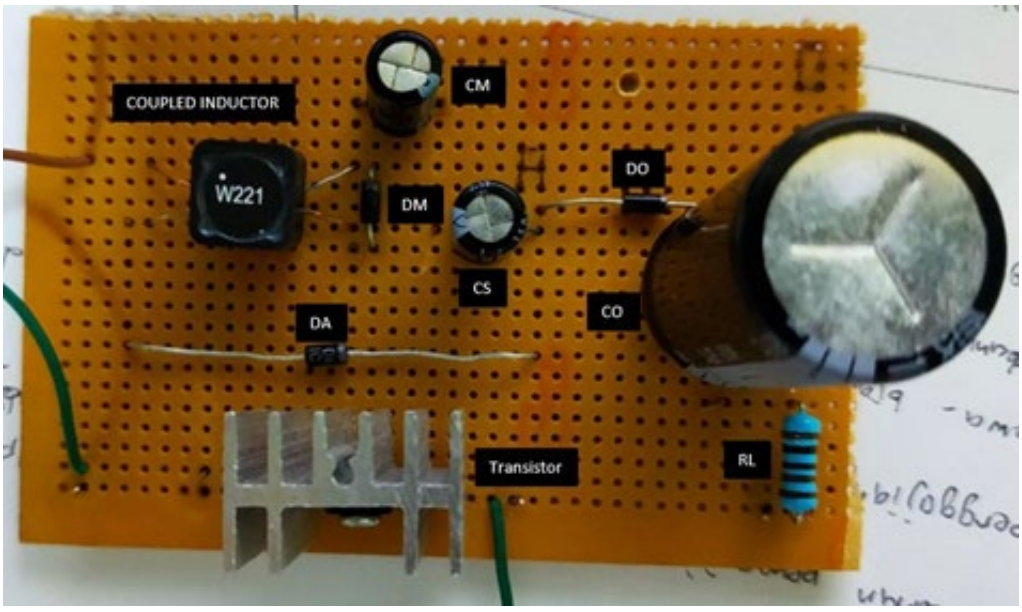

Fig. 12. Prototype of the Proposed Converter

Due to equipment limitation, the switch, L1 & L2 currents of the prototype cannot be measured experimentally. The equipment has no current recording feature built in. However, the equipment can measure the output voltage amplitude and ripple of the proposed converter and they are shown

in Figure 13 and Figure 14. The result of comparison between simulation and experiment of the proposed converter is shown in Table 5.

Table 5
Results Comparison

Data	Simulation	Experimental
Input Voltage	5.0V	4.99V
Output Voltage	18.47V	18.2V
Voltage Ripple	0.0009706V	0.1V
Static Gain	3.694	3.650
Current Switch	0.7476A	Null
L1 Current	0.2780A	Null
L2 Current	0.2096A	Null

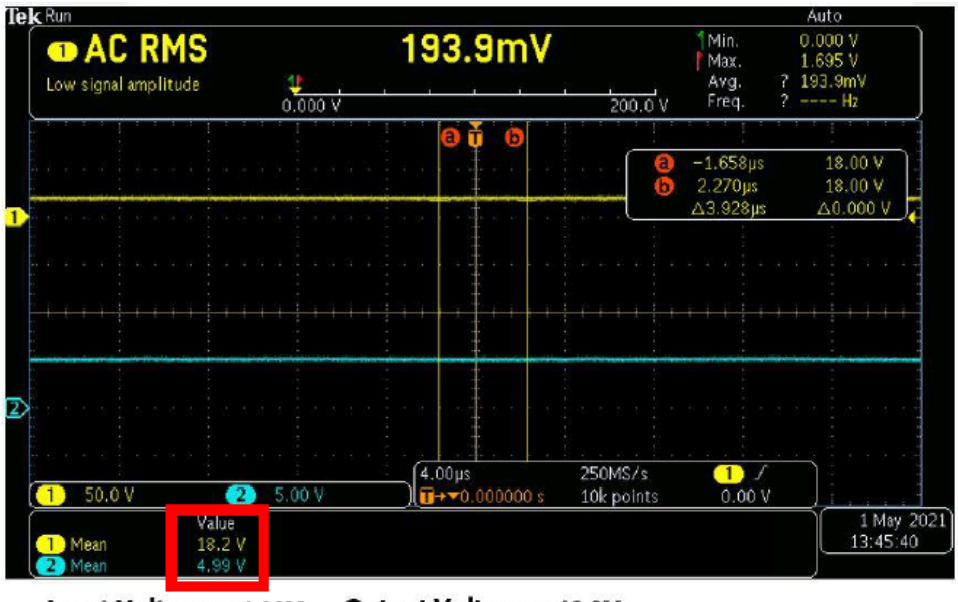

Fig. 13. Experimental Input and Output Voltage Amplitude

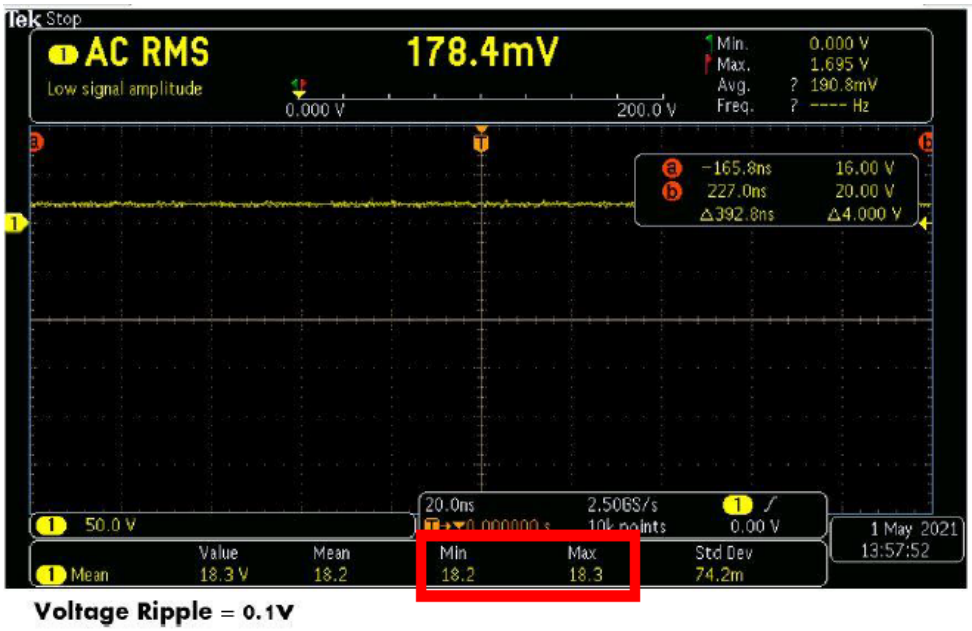

Fig. 14. Experimental Output Voltage Ripple

From the data gathered by simulation and experiment of the proposed converter, it is observed that all the values don't differ much. The percentage of error between the two results is less than 2%. The voltage ripple however shows 99% error when calculated. This is due to simulation software does not have any external noise implemented and therefore, the result is nearly zero. However, the experimental result obtained is 0.1V. That is less than 1% of the output voltage and is considered acceptable. On the other hand, all the currents error percentage value cannot be calculated due to equipment limitation. All the error percentage information is shown in Table 6.

Table 6
Percentage Error

Data	% Error
Input Voltage	0.2%
Output Voltage	1.46%
Voltage Ripple	99%*
Static Gain	1.19%
Current Switch	Null
L1 Current	Null
L2 Current	Null

3.1 Discussion

The proposed converter design is based on the existing topology, Modified SEPIC. The function of inductor in this converter is to store charges during ON & OFF states. Due to the benefits of coupled inductors mentioned in [16], the two uncoupled inductors are replaced with a coupled inductor. The main purpose is to utilize the flux produced by inductor whenever current flows through it. Regardless of any states the converter is at, whenever the current is stored in one side of the uncoupled inductor, the current is always be induced magnetically by the other side of the inductor, contributing to the improvement of the output voltage amplitude. The additional diode, DA is introduced and placed at the input of the secondary side of the coupled inductor to inhibit the reverse current and therefore, reducing the component's stress. Furthermore, the current stability is improved significantly. A prototype of the proposed converter is made to obtain the experimental data for comparison purpose with simulation data. From the results, it is seen that the percentage error between the simulation & experiment is less than 2% which is considered valid. Though the output voltage ripple is having huge percentage error when calculated, but when looking the voltage ripple amplitude value of the experimental data, it is having very minimum value when compared to output voltage amplitude.

As aforementioned, the aim to design a new converter circuit is to improve the performance while having less complexity and less component counts. Although there are lots of research, modelling and prototypes have been made to improve the efficiency of DC-DC converter as published in [17-20], even though the published designs improve greatly, but the circuit complexity is high and requires many additional circuits to trigger the main DC-DC converter circuits.

4. Conclusions

It is analyzed that the proposed design converter performance improves significantly in all aspects when compared to the existing topology, modified SEPIC circuit. It is proven that the circuit can achieve simulation results when conducted experimentally with the percentage of error is less than 2%. It is hoped in the future the currents of switch, L1 & L2 can be measured with the right equipment so the thorough comparison can be made, and the percentage of error can be identified.

Acknowledgement
The authors would like to thank the YUTP 015LC0-419 grant for providing financial support and the department of Electrical and Electronics Engineering, Universiti Teknologi Petronas (UTP), Seri Iskandar, Perak, Malaysia for supporting this research work.

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