SEMARAK ILMU PUBLISHING

Journal of Advanced Research in Applied Mechanics

Journal homepage:
https://semarakilmu.com.my/journals/index.php/appl_mech/index
ISSN: 2289-7895

FPGA-Based Design for Digital Speedometer to Detect Speed Limit of Vehicles

Tan Huat Heng[1], Nabihah Ahmad[1,2,*], Rafidah Ngadengon[1], Phoebe Sia Yun You[1], Arul Edwin Raj Muthu[3]

[1] Department of Electronics Engineering, Faculty of Electrical and Electronics Engineering, Universiti Tun Hussein Onn Malaysia (UTHM), Parit Raja, 86400 Batu Pahat, Johor, Malaysia
[2] VLSI and Embedded Technology (VEST) Focus Group, Universiti Tun Hussein Onn Malaysia (UTHM), Parit Raja, 86400 Batu Pahat, Johor, Malaysia
[3] Department of Electronics and Communication Engineering, Saveetha Engineering College, Chennai, Tamil Nadu 602105, India

ARTICLE INFO

Article history:
Received 1 October 2024
Received in revised form 2 November 2024
Accepted 8 November 2024
Available online 30 November 2024

Keywords:
Digital speedometer; FPGA; speed limit; hall effect sensor

ABSTRACT

This paper presents a proposed design for a digital speedometer using Field Programmable Gate Array (FPGA) technology. The speedometer is a crucial safety feature in vehicles, providing real-time information on the vehicle's speed in kilometres per hour (km/h). The objective of this design is to assist drivers in monitoring and controlling their velocity at regular intervals to ensure safe driving. The hardware platform chosen for implementation is the Altera DE2 Board with Cyclone IV E and the hardware description language used is Verilog HDL. The digital speedometer receives a square wave pulse as an input signal from a hall sensor, which is emitted based on the vehicle's speed. The designed system accurately detects and counts these pulses to convert them into the corresponding speed of the vehicle. This digital speedometer is specifically intended for vehicles with engine capacities (cc) ranging from 1000cc to 1300cc. It can detect speeds within the range of 0km/h to 255km/h. The speed value is displayed on a seven-segment display with precision. Additionally, if the vehicle's speed exceeds the expressway's speed limit of 110km/h, a red LED indicator turns on to alert the driver to control their speed.

1. Introduction

Transportation systems play a vital role in any country and ensuring traffic safety is crucial for their sustainability. One of the most significant challenges faced by many nations is traffic accidents. According to the World Health Organization (WHO) [1], approximately 1.3 million people lose their lives each year due to road traffic crashes. It is important to note that the average speed of vehicles directly impacts both the probability and the severity of accidents. For instance, a mere 1% increase in mean speed leads to a 4% rise in the risk of fatal crashes and a 3% increase in the risk of serious

* *Corresponding author.*
E-mail address: nabihah@uthm.edu.my

https://doi.org/10.37934/aram.127.1.183200

crashes. These statistics highlight the critical importance of managing and regulating vehicle speeds to enhance overall traffic safety.

The Ministry of Transport Malaysia (MOT) and the Malaysian Institute of Road Safety Research (MIROS) [2] have reported significant economic losses for the Malaysian government due to road traffic fatalities. According to the Value of Statistical Life (VSOL) data from 2018 [2], the Malaysian government has suffered losses of at least 3.12 million for each fatality. Furthermore, the frequency of road accidents in Malaysia is a matter of great concern for public health. On average, 18 individuals lose their lives in road accidents every day, highlighting the gravity of the situation. Over the past decade, there has been an alarming increase in the number of traffic accidents, with the reported value of road accidents rising from 414,421 cases in 2010 to 567,516 cases in 2019. These statistics conducted by Ministry of Transport Malaysia [3] underscore the urgent need for comprehensive measures to address road safety and reduce the incidence of accidents in Malaysia.

From the statistics released by Department of Statistics Malaysia [4], road accidents play a significant role in causing death in Malaysia. 2.7% of transport accidents are happened at urban area and 3.3% of transport accidents are happened at rural area in 2020. Most traffic accidents happened in the age groups of 0–14 years, occurring at 3% and the age of 15–40 years group, occurring at 16.8%. According to the data provided by Environment Statistics 2022 [5], the highest number of road accidents in Malaysia occurred in Selangor with 108,564 cases, followed by Johor with 49,559 cases and W.P. Kuala Lumpur with 40,237 cases. Interestingly, when comparing the statistics from Environment Statistics 2021 [6], it is evident that the number of road accidents decreased from 2021 to 2022. This reduction can be attributed to the implementation of the Movement Control Order (MCO) in Malaysia. During the MCO, strict restrictions on movement were imposed, resulting in a significant decrease in overall traffic volume. With fewer vehicles on the road, the likelihood of accidents occurring naturally decreases.

Although the number of traffic accidents have been reduced, the issue about this topic still needs to be focus. Traffic accidents can have severe consequences, including fatalities, serious injuries, mental stress and financial loss. According to Kurnia Insurans [7], speeding is a prevalent factor contributing to road accidents. When drivers exceed the speed limit, their ability to react to unexpected situations diminishes. The impact of a collision in traffic can be fatal for drivers, passengers and pedestrians. Therefore, it is essential to maintain focus on this issue and implement measures to further improve road safety.

In a paper by Papageorgiou *et al.,* [8], a simple model was presented to calculate the number of accidents based on the speed limit. The study revealed an interesting finding that the number of accidents tends to increase as the speed limit increases. This highlights the importance of speed limits in relation to accident rates. Another study conducted by Castillo-Manzano *et al.,* [9] found that a consistent positive association between elevated speed limits and increased traffic fatalities after applying both statistical Fixed and Random Effect Models and heterogeneity analyses.

At the same time, drivers are able to control the vehicle to prevent speeding and avoid accident happen. However, a significant number of them still choose to exceed speed limits and engage in overspeeding. This problem can be attributed to various factors. One frequently mentioned factor is traffic congestion, as drivers feel the need to reach their destinations on time. Additionally, the pressure of being "running late" for work, school, meetings or other appointments is another contributing factor. Despite the risks involved, these factors often lead drivers to prioritize arriving at their destinations quickly, disregarding speed limits and safety precautions.

As to mitigate the occurrence of accidents, speed limit signboards indicating the designated speed are installed at the entry points of restricted speed zones, which are typically areas prone to vehicle accidents. These signboards serve the purpose of reminding and communicating with drivers

by specifying the legal maximum or minimum speed at which vehicles should travel. It is imperative for drivers to adhere to these speed limits and refrain from exceeding the specified maximum speed indicated on the signboards.

Apart from road signboards, the speedometer plays a crucial role in providing drivers with information about the speed and velocity of their vehicles. There are two main types of speedometers: analogue and digital. Analog speedometers feature a smoothly moving needle that can indicate any value within the range of the vehicle's engine capabilities. On the other hand, digital speedometers represent speed values numerically, without the variability of an analogue display.

In this particular project, an implementation of image recognition using Field-programmable Gate Array (FPGA) is employed to detect the speed value from a digital speedometer. According to Rodríguez-Andina *et al.,* [10], FPGA technology allows for algorithm implementation at the hardware level, resulting in faster processing times compared to clock-based processors. Additionally, FPGA enables parallel processing, further enhancing its capabilities for this application.

1.1 Problem Statement

The occurrence of traffic accidents in Malaysia has witnessed a concerning rise in recent years. These accidents have far-reaching negative consequences, including the loss of lives. In particular, accidents involving heavy vehicles tend to result in more severe injuries compared to accidents involving regular vehicles. Zubaidi *et al.,* [11] mentioned that the increased mass of heavy trucks contributes to higher levels of injury severity, as these vehicles require a longer time to slow down and come to a stop. The impact of such crashes can be devastating due to the significant mass involved.

As stated by the Jabatan Pengangkutan Jalan (JPJ) [12], the Automatic Enforcement System (AES) is a tracking system that utilizes sensors installed on the road and an imaging system to automatically record traffic offenses. This system captures photo and video images of traffic violations, with speeding being one of the traffic offenses that are covered by AES.

However, the current implementation of AES on highways in Malaysia lacks the necessary functionality to accurately detect the speed of vehicles. The AES systems deployed on expressways are limited in number, which reduces their overall effectiveness. Additionally, one crucial limitation is that AES is installed at fixed locations. This means that drivers are aware of the exact sites where the AES cameras are positioned, allowing them to anticipate and reduce their speed accordingly to avoid exceeding the speed limit while driving on the expressway.

To address this issue, the development of an efficient system is crucial. A proposed solution involves the creation of a digital speedometer that can accurately detect the velocity of vehicles. This digital speedometer will be designed and implemented on a Field-Programmable Gate Array (FPGA) that can be integrated into the vehicle system. By utilizing a sensor mounted on the vehicle's wheel, the speedometer will detect pulses and calculate the vehicle's speed in kilometres per hour (km/h). The calculated speed will then be displayed on a seven-segment display. The speedometer has the capability to measure speeds ranging from 0 to 255 km/h. Moreover, if the vehicle's speed exceeds 110 km/h, a red LED will be activated to alert the driver. This system aims to provide an efficient and reliable means of monitoring vehicle speed and promoting safer driving practices.

1.2 Speedometer using FPGA

Digital speedometers offer the advantage of directly displaying the numerical speed value, allowing for easy interpretation by drivers. They provide customization options for the visual

representation of speed and the inclusion of additional information such as trip distance or navigation instructions. The large and clear displays of digital speedometers enhance visibility for drivers.

FPGAs, on the other hand, are reconfigurable hardware devices that bring numerous benefits. They can implement any logic function, offer a compact size and consume low power. FPGAs provide portability, reusability, scalability, affordability, parallel processing capabilities and compatibility with various interfaces. They also offer high clock frequency, high operations per second and greater design flexibility compared to ASICs. FPGA technology has found applications in speedometers, automotive instrumentation displays, vehicle speed measurement systems and speed cameras.

FPGA is a flexible hardware device capable of implementing various logic functions. It provides a compact size and low power consumption. FPGA offers several advantages, including portability, reusability, scalability, cost-effectiveness, parallel processing capabilities and compatibility with high or low-level interfaces. It also provides features such as high clock frequency and a high number of operations per second. Additionally, FPGA devices offer the benefit of incorporating security measures.

As mentioned by Boutros and Betz [13], FPGA offer faster design cycles and lower development costs compared to custom-designed chips. The design process of an FPGA architecture involves making various design choices, ranging from high-level architectural parameters to transistor-level implementation details. The objective is to create a highly programmable device while minimizing the area and performance costs associated with reconfigurability.

The primary advantage of FPGAs over Application Specific Integrated Circuits (ASIC) lies in their flexibility. FPGAs have the capability to easily modify their functionality even after the product has been designed. Furthermore, FPGAs can be reprogrammed and reused for different applications or scenarios. They also enable the implementation of complex or innovative logic functions that may not be practical or efficient to achieve with ASIC.

In paper conducted by Aisuwarya *et al.,* [14], the authors discuss the design and implementation of a bicycle's speed measurement system using hall effect sensor. the designed system able to measured speed value, which is obtained by processing the output from a Hall sensor. The sensor detects the magnetic field and sends its signals to the Arduino Uno for further processing. By detecting the pulses, the speed measurement system calculates the speed and the resulting output is then displayed on an LCD display.

Pachorie *et al.,* [15] proposes a design and implementation approach for a digital energy meter using FPGA. According to author, FPGA are well-suited for use in digital speedometers due to their concurrent architecture, reusability and ability to reduce time delays. Unlike microprocessors and microcontrollers, which operate sequentially and can be slower, FPGAs work concurrently, allowing for real-time speed measurements. The reduction in time delay is a result of the concurrent operation of FPGA modules, impacting both processing and communication cycles.

Song *et al.,* [16] proposed a hardware-based Vehicle Speed Measurement (VSM) system using FPGA. The system utilizes a video image technique to measure the speed of a vehicle. The technique involves three steps:

i. generating a background by removing vehicles from a series of captured images using a simplified exclusion algorithm optimized for hardware implementation
ii. subtracting the background from the incoming image and applying affine rectification simultaneously

iii. tracking the vehicles and measuring their velocity based on the rectified image. The system achieved an accuracy of 92.5% in an experiment comparing the measured velocity with the vehicle's speedometer readings.

In a study by Fu and Shi [17], an automatic speed limit enforcement system has been developed for use on freeways, utilizing cameras and Field Programmable Gate Array (FPGA) technology. This FPGA-based system takes advantage of FPGA's parallel processing capabilities to offer a real-time, cost-effective and high-performance hardware platform for multi-channel video systems, enabling real-time image processing. When a speeding vehicle is detected, the system promptly captures panoramic views of the vehicle, its basic characteristics, photographs the vehicle's license plate, records its speed and passing time and transmits this data to a monitoring centre via a wireless modem and GPRS network. Experimental results demonstrate the system's accuracy in detecting vehicle speed and providing evidence for law enforcement purposes.

In this project, opting for a digital speedometer delivers advantages such as accuracy, customizability and improved readability. By utilizing an FPGA for the design, the speedometer can benefit from flexibility, reconfigurability, real-time processing capabilities, low power consumption, cost-effectiveness and compatibility with interfaces and peripherals. These factors make FPGA a suitable choice for developing a digital speedometer with advanced features and optimal performance.

2. Methodology

2.1 Speed Detector System Architecture

The block diagram of the digital speedometer design, as shown in Figure 1, demonstrates how the pulse value from the hall sensor is converted into the corresponding speed value. When a car is in motion, its wheels rotate and this rotation is detected by the hall effect sensor, which senses changes in the magnetic field and generates a square wave output voltage. The frequency of the output square wave is directly related to the speed of the wheel rotation. A higher speed results in a higher frequency and shorter time interval between successive pulses.

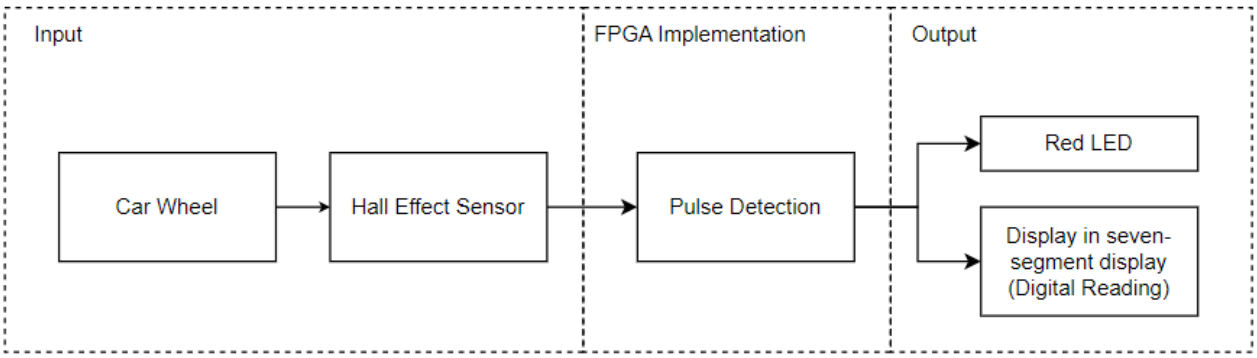

Fig. 1. Block diagram of design for digital speedometer

The output voltage from the hall effect sensor serves as the input signal for the FPGA implementation. The FPGA processes the pulse detection, utilizing two counters to keep track of the number of pulses and determine the speed of the vehicle. The calculated speed value is then displayed on a seven-segment display in a digital format. Additionally, if the speed of the vehicle exceeds 110 km/h, the Red LED is activated as a visual alert.

Figure 2 illustrates the working principle of a wheel speed sensor in conjunction with a hall effect sensor. As stated by Dejan [18], the hall effect sensor is positioned near a magnet, which generates a magnetic field. As the wheel rotates, the magnetic field undergoes changes in strength or polarity. The hall effect sensor detects these magnetic field variations and converts them into electrical signals. This sensor operates based on the hall effect phenomenon, which refers to the voltage difference across a conductor when exposed to a magnetic field. As the wheel rotates, the changing magnetic field causes a corresponding change in the voltage output of the hall effect sensor.

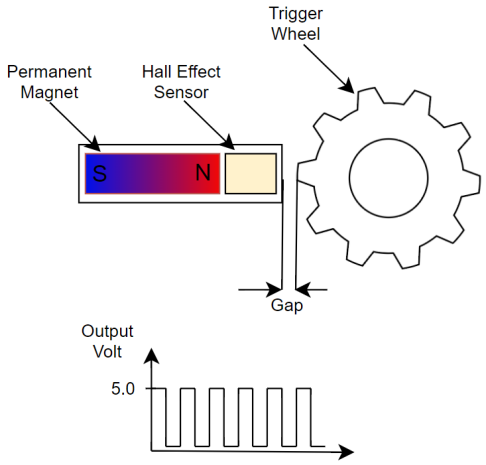

Fig. 2. Working principle of hall sensor

The hall effect sensor is positioned in close proximity to the teeth or notches on a disk attached to the wheel. As a tooth passes near the sensor, the magnetic field experienced by the sensor changes, resulting in a switch between high and low voltage states in the sensor's output. This produces a square wave signal with a specific frequency that corresponds to the rotation of the wheel. By analysing the frequency of the square wave signal, the rotational speed of the wheel, measured in revolutions per minute (RPM), can be determined. Fowler [19] introduces the square wave signal with varying frequencies, which can be utilized to distinguish between low-speed and high-speed wheel rotation, as depicts in Figure 3.

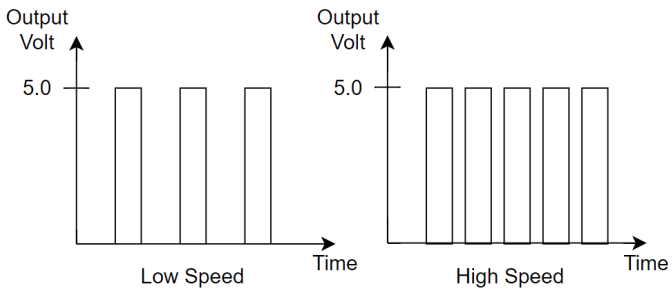

Fig. 3. Square wave with two different frequencies

The Altera DE2 Board, equipped with Cyclone IV E, is the fundamental hardware platform that provides the processing power needed to run the digital speedometer. Its Cyclone IV E FPGA makes it possible to execute complicated algorithms and integrate a variety of components, both of which are essential for precise speed detection. In addition, the hardware level modelling of the speedometer is greatly aided by the usage of Verilog HDL. Verilog makes it easier to design, simulate, synthesise and implement the system on the FPGA. This guarantees a thorough representation of behaviour and makes development, testing and deployment more efficient. The synergy between

the hardware platform and Verilog HDL boosts the reliability and performance of the digital speedometer, offering a stable foundation for real-time speed monitoring.

The digital speedometer design is tailored for vehicles with engine capacities ranging from 1000cc to 1300cc, ensuring precise speed measurements. This targeted range enhances precision within the 0-255 km/h speed range, contributing to safer driving practices. The system's scalability considerations allow for potential adaptations to accommodate varying engine capacities, providing flexibility to meet the specific speed measurement needs of different vehicles.

2.2 Proposed Digital Speedometer Operation

The operation of the digital speedometer can be summarized as counting the number of changes in the magnetic field detected by the hall effect sensor within a specific time period. The digital speedometer receives a square wave pulse as an input signal from hall sensor, which is emitted based on the vehicle's speed. The square wave signal is generated by the hall effect sensor as the teeth or notches on a disk attached to the wheel pass near the sensor, causing changes in the magnetic field experienced by the sensor. This results a switch between high and low voltage states in the sensor's output, producing a square wave signal with a specific frequency corresponding to the rotation of the wheel. Figure 4 depicts the flow chart illustrating the operation of the speed detector's counter.

In Phase 1, the operation begins by initializing both the clock counter and the hall effect sensor counter. The clock counter is responsible for counting the number of clock cycles to determine the specific time duration. On the other hand, the hall effect sensor counter is used to track the number of changes in the magnetic field detected by the hall effect sensor during that time.

Moving on to Phase 2, the pulse detection process is initiated once the counters have been properly initialized. By obtaining the number of pulse detections, this value is then utilized to calculate the speed using the Eq. (1) as outlined in the reference [12].

$$V = \frac{C \times N}{T} \times 3.6 \tag{1}$$

where the speed in unit km/h, V, circumference of the wheel in unit meter, C, number of pulses detected in particular time, N and particular time in unit second, T.

In Phase 3, the calculated speed value is displayed on a seven-segment display with precision, providing real-time information to the driver. The digital speedometer system utilizes the seven-segment display to visually represent the calculated speed value in a digit-based format. The display consists of three digits: ONES, TENS and HUNDREDS, represented by HEX0, HEX1 and HEX2, respectively. Each digit is illuminated using a combination of segments, allowing for the clear representation of numerical values from 0 to 9. The precision or resolution of the display enables the accurate conveyance of the vehicle's speed within the range of 0km/h to 255km/h. This high-resolution display ensures that the driver can quickly and easily assess the current speed of the vehicle, contributing to safe driving practices. Additionally, a comparison is made between the calculated speed value and a predefined threshold, such as 110 km/h. If the calculated speed exceeds this threshold, the red LED indicator is activated to alert the driver.

The proposed digital speedometer, leveraging FPGA technology, not only ensures user-friendly features but also exhibits potential for seamless integration into existing vehicle dashboard systems. Accurate speed display via a seven-segment display enhances user-friendliness, while the red LED indicator, signalling speeds exceeding 110km/h, promotes safe driving. Considerations for compatibility with diverse interfaces, alongside portability and reusability facilitated by FPGA

technology, make this digital speedometer a practical choice for enhancing vehicle instrumentation and encouraging responsible driving practices.

3. Results

3.1 Simulation Result of Digital Speedometer

The simulation setup for the speedometer system utilizes an input clock frequency of 50 MHz. To achieve a desired duty cycle of 0.5 seconds, a clock divider is employed to divide the frequency accordingly. This division ensures that the speedometer system in the simulation refreshes its results every 0.5 seconds. By updating the displayed speed at regular intervals, the speedometer provides an accurate and reliable measurement of speed. The output simulation waveforms, generated using the "Modelsim Altera" tool in Intel Quartus Prime software.

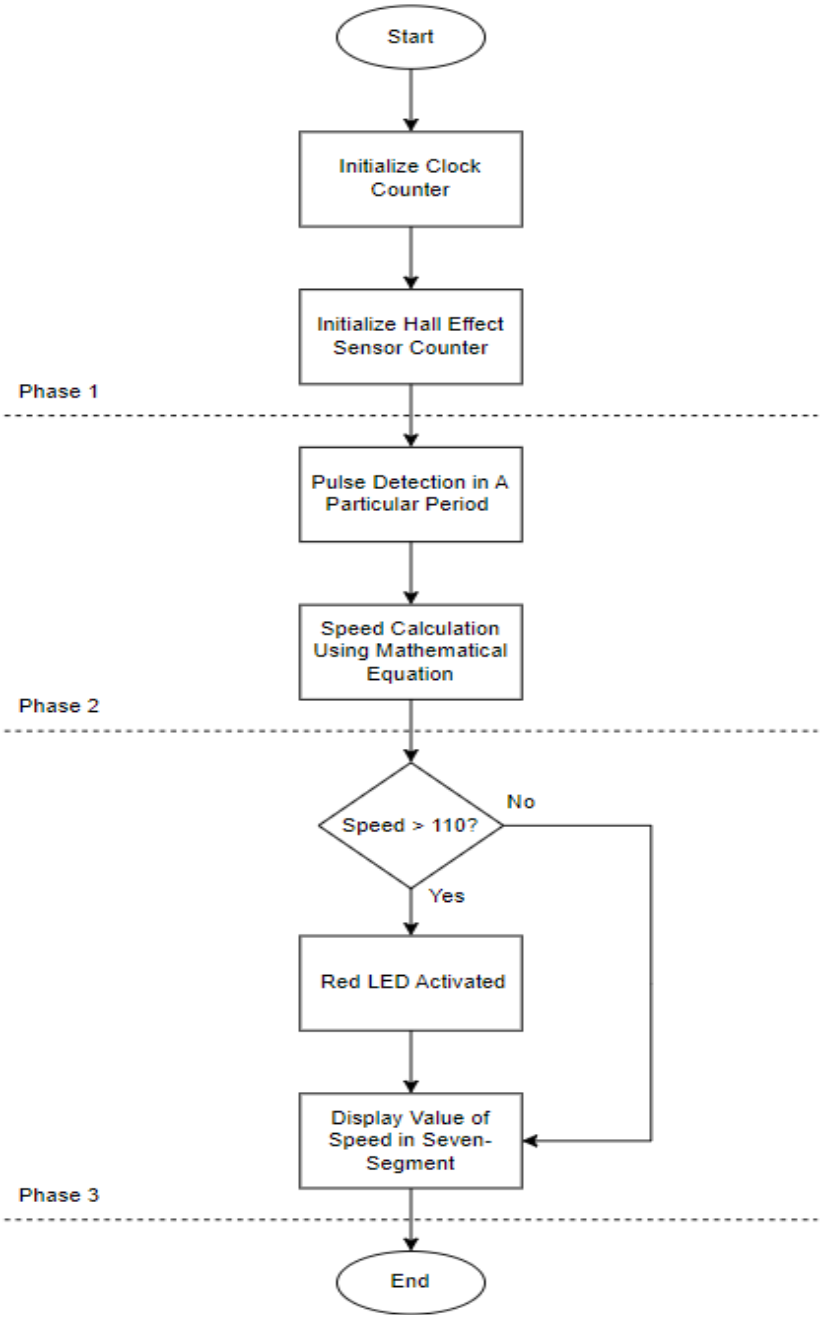

Fig. 4. Flow chart for the operation counter of speed detector

Figure 5 illustrates a simulation result where the speed remains below 110 km/h. The simulation ran with a duty cycle of 0.5 seconds, as indicated by the "clk" signal. Within this interval, the "counter" records a total of 150 inputs from the hall effect sensor. After processing these inputs, the resulting value of 86 is displayed on the seven-segment display. In the simulation, the seven-segment display labelled as "HEX2" shows the digit "0" represented by the binary number 1000000. The seven-segment display labelled as "HEX1" displays the digit "8" with the binary number 0000000, indicating that none of the segments are illuminated. Lastly, the seven-segment display labelled as "HEX0" displays the digit "6" represented by the binary number 0000010. As the speed value of 86 does not exceed the speed limit of 110 km/h, the red LED, represented by the "red_led" output, remains inactive in this scenario.

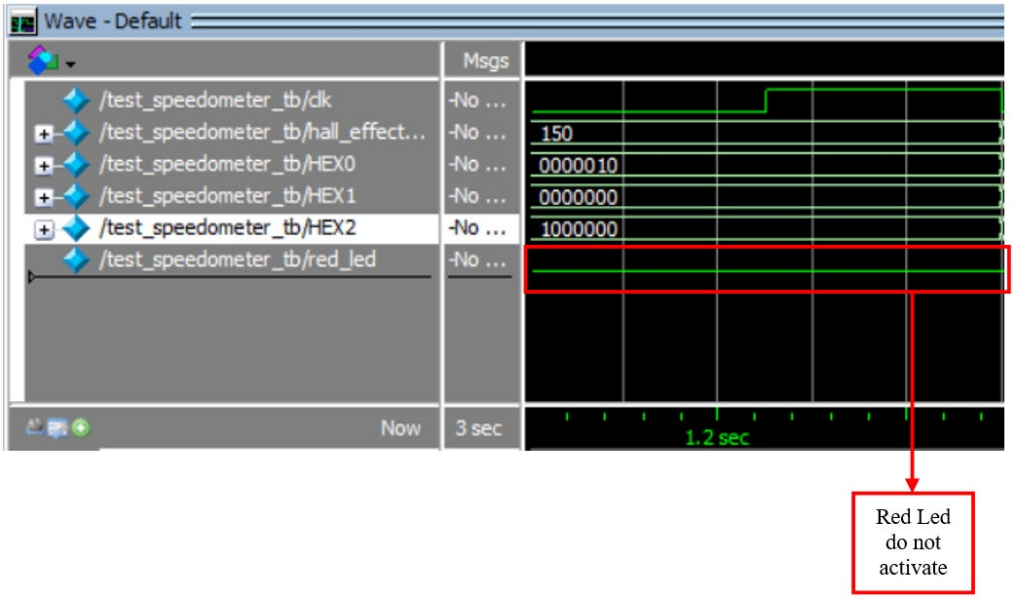

Fig. 5. Simulation result below 110km/h

In Figure 6, the simulation result demonstrates a speed above 110 km/h. Within the 0.5-second interval, the counter counts a total of 200 inputs from the hall effect sensor. After processing these inputs, the resulting value of 115 is displayed on the seven-segment display. The seven-segment display labelled as "HEX2" shows the digit "1" represented by the binary number 1111001. Similarly, the seven-segment display labelled as "HEX1" also displays the digit "1" with the binary number 1111001, indicating that none of the segments are illuminated. Lastly, the seven-segment display labelled as "HEX0" displays the digit "5" represented by the binary number 0010010. As the speed value of 115 exceeds the speed limit of 110 km/h, the red LED, represented by the "red_led" output, becomes activated in this scenario.

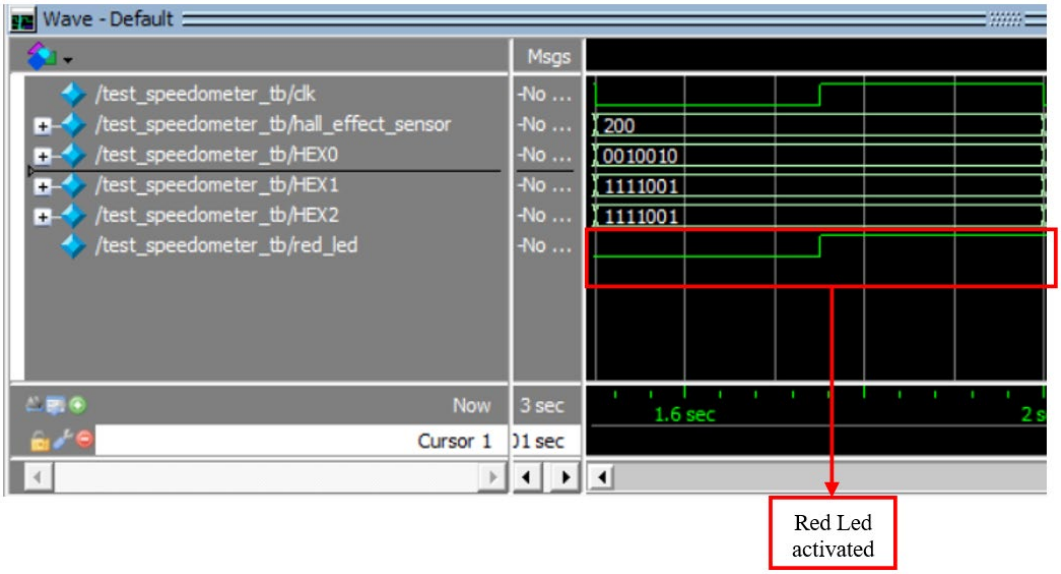

Fig. 6. Simulation result above 110km/h

Table 1 presents the segment control and their corresponding hexadecimal equivalent binary numbers for the Seven-Segment Displays.

Table 1
Corresponding numbers on single seven-segment display

Digit	G	F	E	D	C	B	A	HEX [6:0]
0	OFF	ON	ON	ON	ON	ON	ON	100 0000
1	OFF	OFF	OFF	OFF	ON	ON	OFF	111 1001
2	ON	OFF	ON	ON	OFF	ON	ON	010 0100
3	ON	OFF	OFF	ON	ON	ON	ON	011 0000
4	ON	ON	OFF	OFF	ON	ON	OFF	001 1001
5	ON	ON	OFF	ON	ON	OFF	ON	001 0010
6	ON	ON	ON	ON	ON	OFF	ON	000 0010
7	OFF	OFF	OFF	OFF	ON	ON	ON	111 1000
8	ON	ON	ON	ON	ON	ON	ON	000 0000
9	ON	ON	OFF	ON	ON	ON	ON	001 0000

Jensen [20] demonstrates the definition of each segment (A, B, C, D, E, F and G) on the display, as illustrates in Figure 7. By controlling the state of each segment using a single bit, different combinations of illuminated segments can represent numbers from 0 to 9, as well as certain characters such as A, B, C, D, E, F and G. The table showcases the output segment configuration for each display along with its associated binary number in hexadecimal format. This arrangement enables the effective representation and clearly conveys various digits and characters on the Seven-Segment Displays.

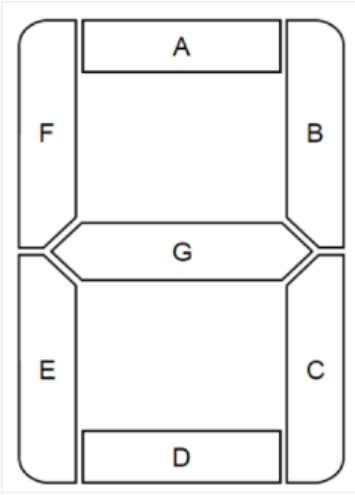

Fig. 7. Segment seven-segment display

Figure 8 to Figure 12 shows RTL Viewer Designed Speedometer. It provides a graphical representation of the design hierarchy, with the top-level module being "fina_speedometer" and containing seven submodules ("add3:m1", "add3:m2", "add3:m3", "add3:m4", "add3:m5", "add3:m6" and "add3:m7".

Figure 8 depicts Part A of the RTL Viewer Designed Speedometer, which consists of two inputs: hall_effect_sensor and CLOCK_50. Firstly, the blocks counter_h, counter_nd and kali are utilized to count the number of changes in the detected magnetic field. Secondly, the counter acts as a clock divider when driven by the CLOCK_50 input. This division of the clock frequency generates smaller frequencies that are used within the designed system and the resulting divided clock frequency is provided as the clock_out output.

In Figure 9, Part B of the RTL Viewer Designed Speedometer is displayed. This section focuses on the mathematical calculations related to speed, involving arithmetic logic operations. For example, the Add3 and Div0 blocks are employed in this part to perform speed calculations.

Figure 10 and Figure 12 presents the parts that manage the logic required for displaying the velocity value on a seven-segment display. The display consists of three digits: ONES, TENS and HUNDREDS, represented by HEX0, HEX1 and HEX2, respectively. Figure 11 involves the development of seven submodules named "add3:m1," "add3:m2," "add3:m3," "add3:m4," "add3:m5," "add3:m6," and "add3:m7." Each of these submodules comprises registers, logic blocks and interconnections. Their purpose is to convert the speed value into three digits: ONES, TENS and HUNDREDS. These submodules work together to enable the appropriate representation of the speed on the seven-segment display.

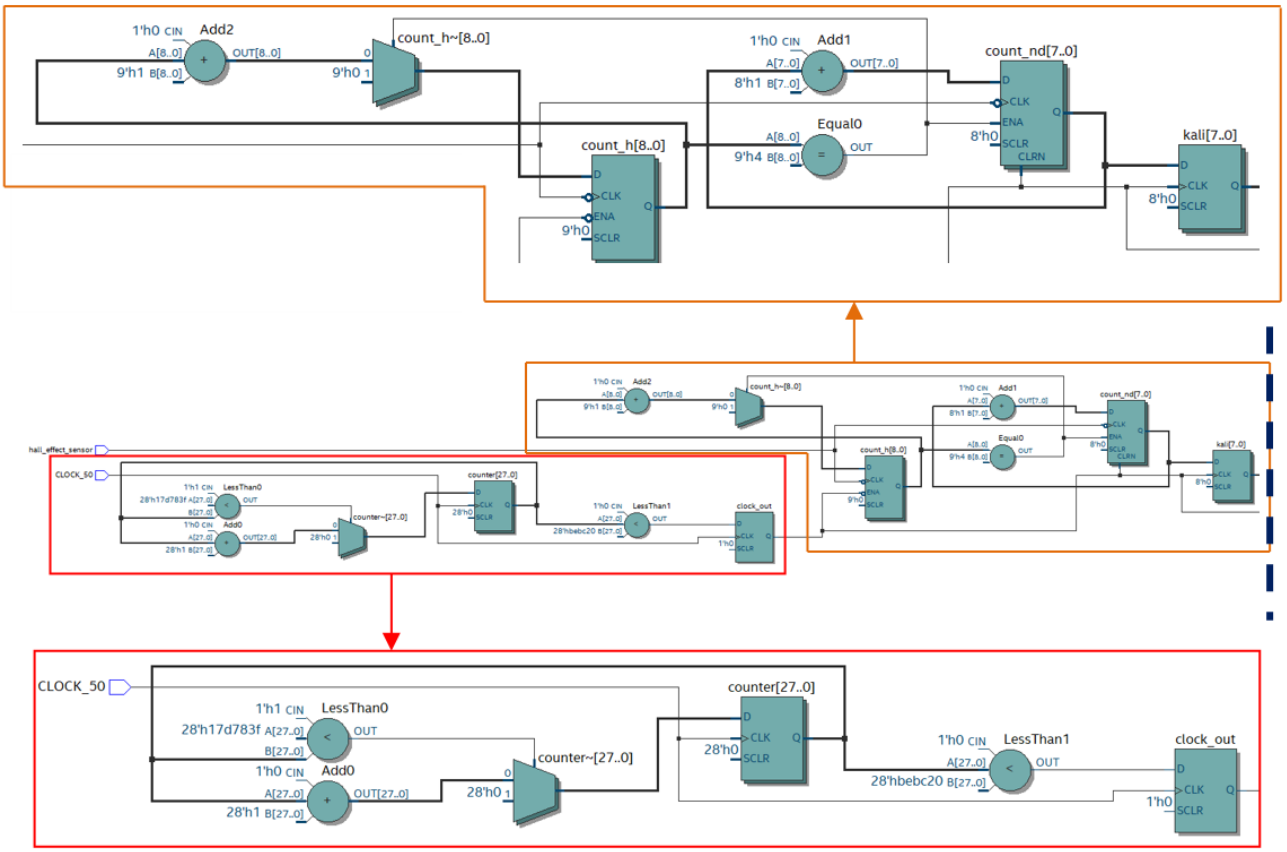

Fig. 8. RTL viewer designed speedometer Part A

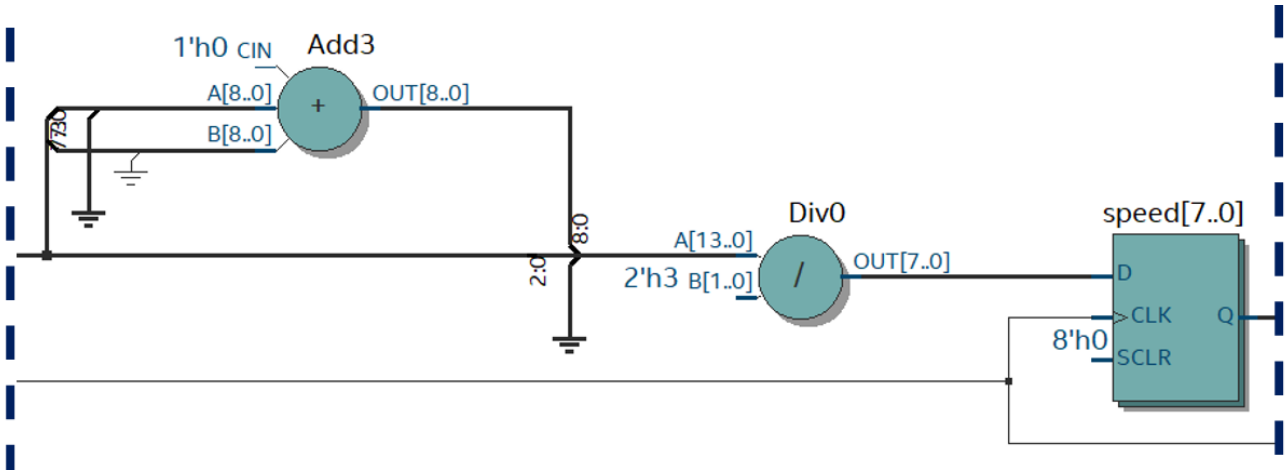

Fig. 9. RTL viewer designed speedometer Part B

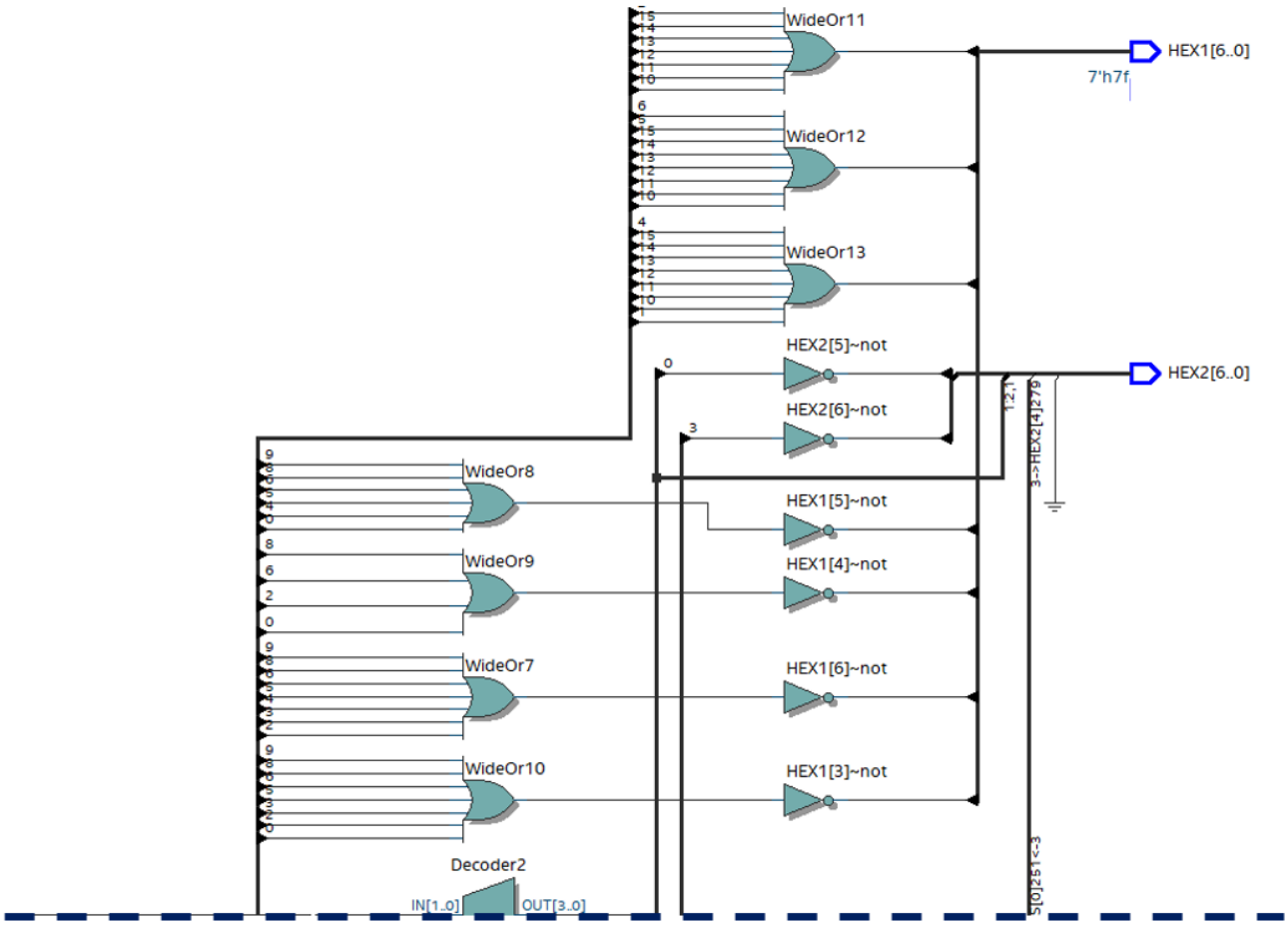

Fig. 10. RTL viewer designed speedometer Part C

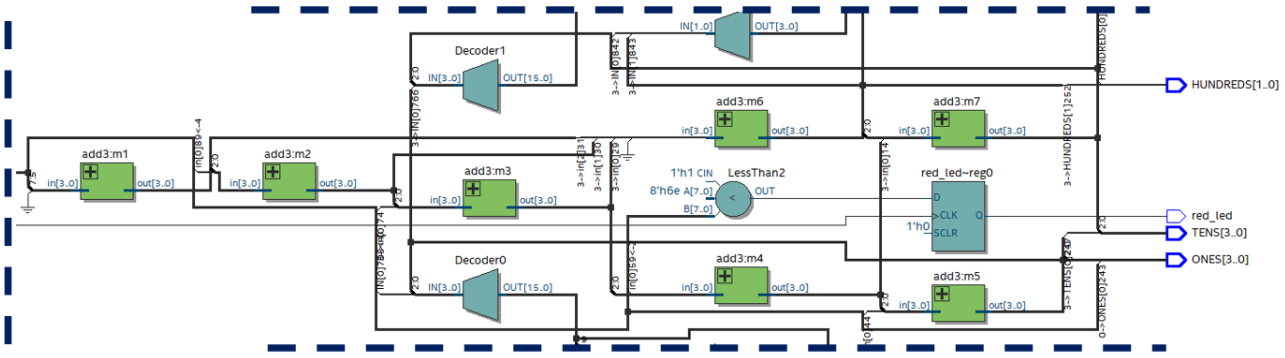

Fig. 11. RTL viewer designed speedometer Part D

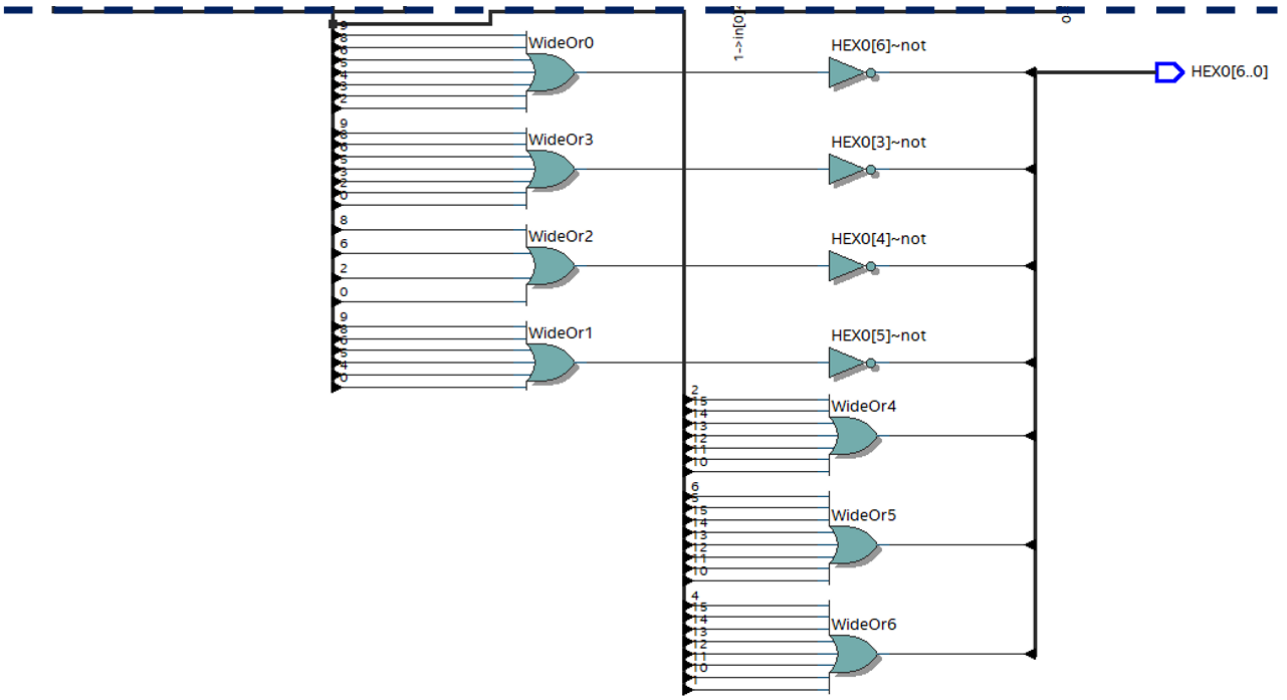

Fig. 12. RTL viewer designed speedometer Part E

3.2 Prototype of Digital Speedometer

Figure 13 showcases a prototype of the designed speedometer system. The prototype consists of several components, including an FPGA board, an Arduino car, a Hall effect sensor, a seven-segment display and a red LED.

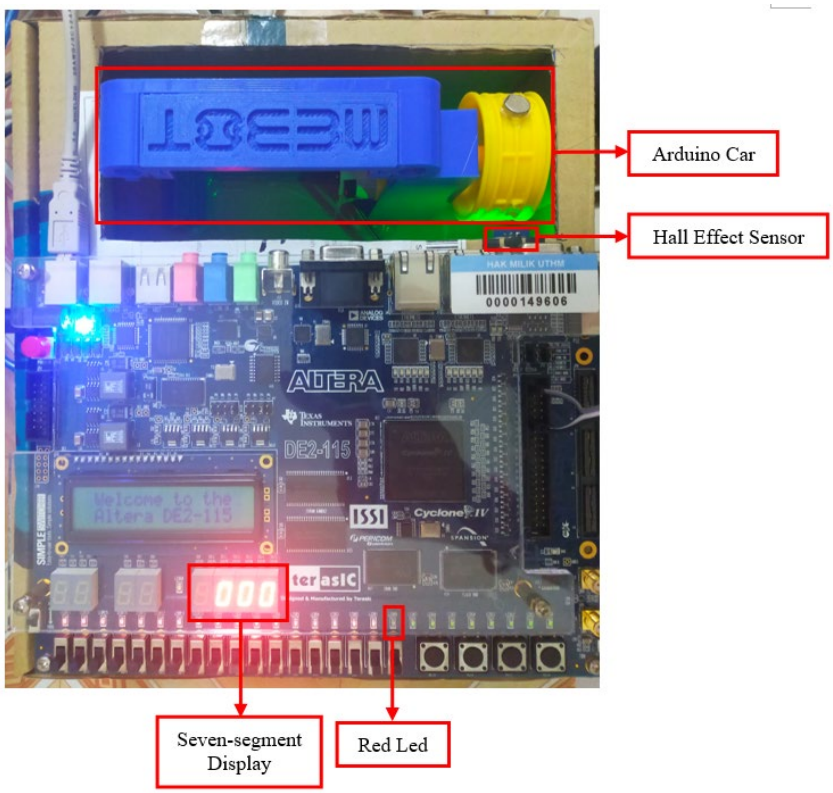

Fig. 13. Prototype designed speedometer

The Arduino car serves as a small robotic vehicle that incorporates DC motors, a motor driver and a chassis, allowing it to move. The Arduino microcontroller board acts as the control unit, receiving input signals and generating output commands to control the car's motion and operate the motors.

To accurately measure the speed of the car's rotating wheels, a Hall effect sensor is utilized. This sensor utilizes the Hall effect principle to detect changes in the magnetic field caused by a rotating magnet or trigger wheel, enabling precise speed measurements.

The prototype includes a seven-segment display, which visually presents the speed information in a digit-based format. This display allows for the clear representation of the speed measured by the Hall effect sensor, providing the driver with a visual indication of the current speed.

Furthermore, a red LED is integrated into the prototype as a visual indicator. In the described speedometer system, the red LED would activate when the car's speed exceeds a predetermined limit, serving as a reminder for the driver to reduce their speed and promoting safer driving practices. This feature is crucial for enhancing safety on the road, it provides a clear and immediate indication to the driver when the vehicle's speed exceeds the permissible limit.

3.3 Result Designed Speedometer on FPGA Board

Figure 14 illustrates a scenario where the wheel's speed is below the defined speed limit of 110 km/h. In this situation, the red LED in the prototype remains inactive, indicating that the current speed is within the acceptable range.

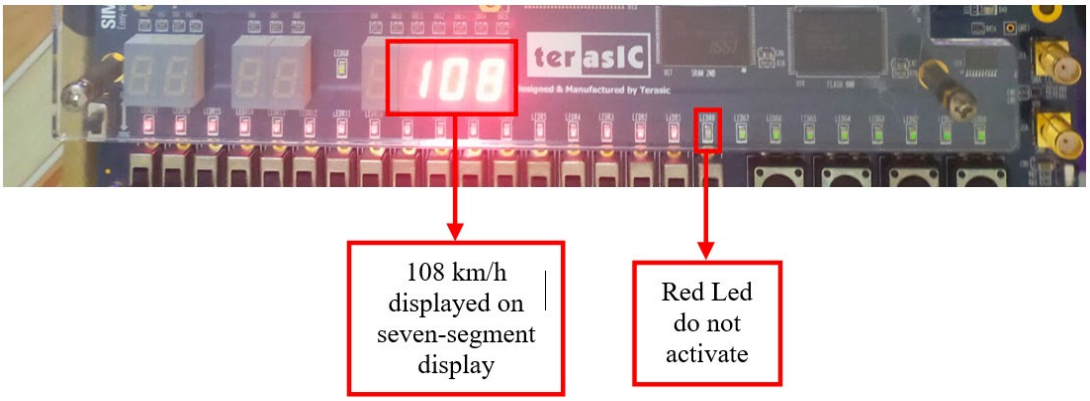

Fig. 14. Result when the wheel is turn at speed below 110km/h

In contrast, Figure 15 depicts a different scenario where the wheel's rotation speed exceeds the defined speed limit of 110 km/h. As a result, the red LED in the prototype becomes active, functioning as a visual reminder for the driver to reduce their speed while driving.

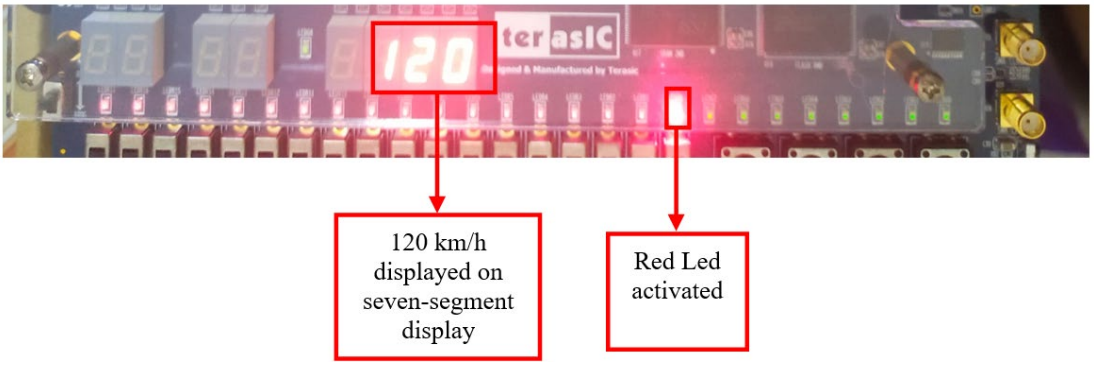

Fig. 15. Result when the wheel is turn at speed above 110km/h

3.4 Power Analysis and Resource Usage

The power consumption of the top-level module is analysed and shown in Figure 16. The total Thermal Power Dissipation for the speedometer system via FPGA implementation is 142.95mW. The Core Static Thermal Power Dissipation is 98.50mW and Input Output Thermal Power Dissipation is 44.45mW.

Quartus Prime Lite is used to synthesize RTL design for the FPGA. The percentage of hardware resources required for designed speedometer using FPGA implementation is shown in Figure 17.

PowerPlay Power Analyzer Summary

<<Filter>>

PowerPlay Power Analyzer Status	Successful - Fri Jun 09 11:35:07 2023
Quartus Prime Version	17.0.0 Build 595 04/25/2017 SJ Lite Edition
Revision Name	fina_speedometer
Top-level Entity Name	fina_speedometer
Family	Cyclone IV E
Device	EP4CE115F29C7
Power Models	Final
Total Thermal Power Dissipation	142.95 mW
Core Dynamic Thermal Power Dissipation	0.00 mW
Core Static Thermal Power Dissipation	98.50 mW
I/O Thermal Power Dissipation	44.45 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data

Fig. 16. Power Analyzer Summary of designed system

Fitter Summary

<<Filter>>

Fitter Status	Successful - Fri Jun 09 11:34:24 2023
Quartus Prime Version	17.0.0 Build 595 04/25/2017 SJ Lite Edition
Revision Name	fina_speedometer
Top-level Entity Name	fina_speedometer
Family	Cyclone IV E
Device	EP4CE115F29C7
Timing Models	Final
Total logic elements	204 / 114,480 (< 1 %)
Total registers	61
Total pins	41 / 529 (8 %)
Total virtual pins	0
Total memory bits	0 / 3,981,312 (0 %)
Embedded Multiplier 9-bit elements	0 / 532 (0 %)
Total PLLs	0 / 4 (0 %)

Fig. 17. Summaries of the hardware resource usage

3.5 Comparison with Previous Work

Table 2 presents a comparison between the proposed design in this project and reference works [14,16,17]. It is observed that the proposed digital speedometer achieved lower accuracy compared to the mentioned reference works.

In reference work of Song *et al.,* [16], the system utilized a video image technique to measure the speed of the vehicle. In contrast, the proposed design employed a hall effect sensor to detect changes in the magnetic field. It is likely that limitations in the design and implementation of the proposed system affected its accuracy, leading to the observed differences in performance compared to the reference works. The proposed design achieves an area utilization of 1% when implemented in Quartus Prime software.

Table 2
Comparison between proposed design and reference work

Author	Year	Method	Board	Accuracy	Area
[14]	2019	Detection of magnetic field using hall sensor	Arduino Uno	-	-
[17]	2010	Image processing algorithm	ALTERA Cyclone EPIC12 FPGA	-	-
[16]	2010	• Background image creation and subtraction • Image rectification • Vehicle detection and tracking	-	92.5%	-
Proposed Design	2023	Detection of magnetic field using hall sensor	DE2-115	83.74%	1%

The digital speedometer, designed with FPGA technology, offers flexibility to accommodate diverse speed limits globally. The design and implementation of the digital speedometer encountered challenges related to achieving accuracy and performance comparable to previous works. The proposed system faced limitation that affects its accuracy, leading to lower performance. These challenges were tackled by incorporating a hall effect sensor for detecting magnetic field changes and leveraging FPGA technology to achieve real-time processing and precise speed detection. Its FPGA-based design allows reconfigurability and scalability, enabling adjustments to speed thresholds and visual alerts, like the red LED, in accordance with regional regulations. The use of Verilog HDL allows implementation of logic functions, ensuring adaptability to different speed limit requirements, promoting road safety and compliance with local regulations across various regions or countries.

4. Conclusions

In conclusion, the implementation of the FPGA-based speedometer system has successfully achieved its goal of accurately detecting the wheel's speed. By utilizing the Altera DE2-115 board with the Cyclone IV E family and the EP4CE115F29C7 device, the system has been able to leverage the computational power necessary for its operations.

A notable feature of the system is the activation of the red LED, which serves as a reminder to the driver when the speed exceeds the predetermined limit of 110 km/h. This feature enhances safety by prompting the driver to reduce their speed, promoting responsible behaviour on the road.

Additionally, the system incorporates a seven-segment display that effectively visualizes and displays the calculated velocity value. This display provides clear and easily understandable information to the driver, enabling quick assessment of the current speed.

Throughout the project, the Quartus Prime Lite software played a vital role in simulating and programming the FPGA board. This software offered a comprehensive set of tools and capabilities, ensuring efficient development and testing of the speedometer system.

Regarding power consumption, the designed system demonstrates a power usage of 142.95mW. This information is crucial for understanding the energy requirements of the system and can be utilized for future optimization and considerations related to power efficiency.

To summarize, the FPGA-based speedometer system has successfully achieved accurate speed detection. The activation of the red LED and the display of velocity value on the seven-segment display provide valuable feedback to the driver. The integration of the Altera DE2-115 board, Cyclone IV E family and EP4CE115F29C7 device, along with the utilization of Quartus Prime Lite software, has facilitated the development of a reliable and efficient system. The recorded power consumption of 142.95mW provides insights for further enhancements and optimizations in future iterations of the system.

Acknowledgement

This research received no specific grant from any funding agency in the public, commercial or not-for-profit sectors.

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