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Review Article: Voltage Balancing Method for Battery and Supercapacitor as Energy Storage

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ABSTRACT

This paper examines several existing voltage equalizers techniques for energy storage system, with a focusing on batteries and supercapacitors. Due satisfy the demands, energy storage cells are often coupled in series/parallel. However, divergence of voltage distributed among cells produces the problems of voltage imbalance that affecting the ageing of energy storage system and solved through equalizers. Several assessments from features of topologies in voltage balancing circuit supplied primarily based total on a few attentions' just like the effectiveness in balance and components. Voltage balancing is essentially separated into two categories: passive and active equalizers. Therefore, this paper studied and reviewed several topologies from both equalizer types with the sample result to verify the topology performance.

1. Introduction

Nowadays, developments in energy storage system become the biggest challenge in the world. Since consumers need to follow up the headway is a must. Development of environmentally friendly electric vehicles, noise-free become an attraction to people. The predicted electric vehicle market will reach 27 million units by 2030 [1]. Indirectly, the storage system is the source of most issues in an electric car. The capacity and reliability of the storage system that can cover the kilometers after one charge are being investigated to solve user anxiety. Batteries were the first energy storage device employed in an electric car, capable of producing long-term driving energy. Short-term power loads faced during quick accelerations and regenerative brake decelerations, on either side, are also the limitations [2]. Additionally, the battery is also having a heavyweight with a large volume. Consequently, leading to another problem which time to recharge is longer. Another alternative takes with supercapacitor as an option for a storage system. Supercapacitors (SCs), also known as Ultracapacitors (UC), compromise on pumping the complete power to the load in seconds. SCs have

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recently been prominent in a variety of applications because inherent benefits such as power system protection, ride-through, and transmission with distribution stability [3]. Additionally, SCs also provide a long lifetime, better efficiency, and dynamic response also higher capacitance [4].

SCs are classified as electric double-layer capacitors (EDLC), pseudocapacitors, or hybrids [5]. The foremost commercial SCs that fits the large scale of energy storage is EDLC. The structure of SCs arranges in series. Factors like internal parameters in SCs (capacitance, Equivalent Series Resistor (ESR) caused the cells of SCs to create voltage unbalance problems. Furthermore, other drawbacks with supercapacitors are having low-rated voltages which limited range in each cell (0 – 2.7V) [6]. About 14 V is needed for automotive applications by having six individual SCs cells [7]. Effects of this problem bring SCs unable to supply the energy capacity as required since the difference in operational voltage in different cells. The lifetime and reliability of the system also will be an influenced. As a result, determining the way of balancing initiatives to enhance capacitance is necessary. By following, this research also brief overview of different topologies in voltage balancing/equalizers can be observed which have been summarized in Figure 1. These different topologies presented which involved two types which are passive equalizers and active equalizers. There are several previous research names these passive equalizers are sometimes referred to as dissipative cell/voltage balancing, while active equalizers are referred to as non-dissipative cell/voltage balancing. Furthermore, a path comparison of the equalization topologies given has been demonstrated and concluded.

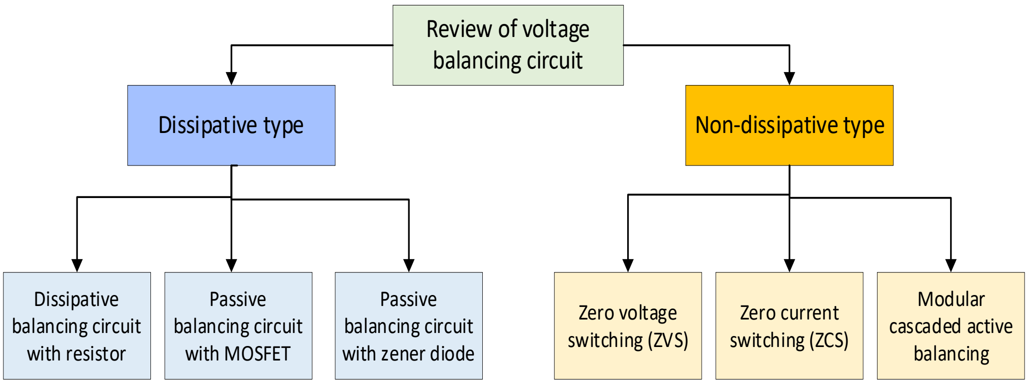


Fig. 1. Different topology of review equalizers

2. Voltage Equalizers

Considering single cells of batteries and supercapacitors have low voltage rates, they must be connected in series and parallel to provide the requisite energy storage capacity across each application. However, voltage distribution varies due to varied characteristics issue such as capacitance, equivalent series resistance (ESR), and self-discharge rating in different cells, that all impact supercapacitor dependability. As a result, the SC balance circuit was constructed based on several characteristics presented using various topologies.

2.1 Energy Storage Voltage Balancing Method

Some of the topologies chosen with various kinds have been changed and discussed in order to identify the best way depending on applications. The techniques utilized to balance the voltage cell are passive and active equalizers.

2.1.1 Passive voltage balancing

The passive circuit is comprised of resistors, inductors, and other devices that assist in the balancing of the cell banks. This circuit's balancing circuit eliminates surplus charge from highly charged cells. Because of its simplicity and low cost, the passive balancing circuit is still commonly used in the market [8]. The circuit constructed is also bulky and expensive with heat sinks.

The classical structure of passive equalizers has been considered known as switched shunting resistor [9]. The system is simple, consisting of a series of SC cells with parallel equal resistors and switches. Due to the shunting resistor generates an inaccurate value, the cells overcharge, lowering SC lifespan. To achieve the voltage equalizers, switched attach to cells shunting resistor to put ON/OFF manage the charging current [8]. To recap, retain the charging shunting switch switched off until the voltage cell terminal reaches the rated voltage. However, because to cell disparity, certain cells reach rated voltage early, leaving the system unable to cease charging. As a result, the shunting switch turns on when the ready charges in the shunting resistor are transferred at a slow speed until the full charging condition is reached. However, the slowest speed issue occurs in the shunting resistor, which causes shunting to be turned off. To solve quicker fast - charging time, a switched resistor balancing circuit passive equalization was created. To summaries the procedure, maintain the charging shunting switch turned OFF until the voltage cell terminal achieves the rated voltage. However, because to cell disparity, certain cells reach rated voltage early, leaving the system unable to cease charging. As a result, the shunting switch turns on when the ready charges in the shunting resistor are transferred at a slow speed until the full charging condition is reached. However, the slowest speed issue occurs in the shunting resistor, which causes shunting to be turned off. To solve quicker fast charging time, a switched resistor balancing circuit passive equalization was created. Ahmad *et al.,* [10] introduced two topologies of passive equalizers fixed shunting and switching shunting resistor where the feature be reported in Table 1.

Table 1
Passive equalizers categories [10-13]

Types	Description	Advantages	Disadvantages
Fixed shunting resistor	Using continuous bypassing the current for all cells and cell voltage being adjusted by resistor	Simplicity Low cost	Only can be used for lead-acid and Nickel-based batteries. Permanent energy loss and does not have controlled operation.
Switching shunting resistor	Not continuous since removing the energy from higher cells and controlled by switches/relay	Could be in two modes (Continuous mode and detecting mode) Reliable (can be used for Li-ion batteries)	Having excess energy from higher cells becomes dissipated when heat. If applied during discharge shorten the battery time.

The Cockcroft-Walton (CW) voltage multiplier is another type of passive equalization. This model is made up of a diode-capacitor that generates numerous uniform output voltages while needing fewer switching and/or transformer windings [14]. The advantage of CW is that it simplifies the initial suggested task of the DC-DC multilevel boost converter. Diodes and capacitors minimize cost and power switching indirectly. The disadvantage of CW is that when turned on, a huge arriving current travels through the capacitor, causing damage to the parallel capacitor. Thus, a modified voltage equalizer was introduced to avoid partial unbalance voltage cells adding the half bridged into the circuit [14]. The half-bridge produces a square wave that can observe the current flow in or out at SCs through when CW as a voltage equalizer.

2.1.2 Active voltage balancing

Excess charge from higher voltage energy storage cells is redistributed to lower voltages through active balancing circuits. Generally, active equalizers accomplish the recovery of optimal energy distribution [15]. These type categories under different groups known as adjacent cell to cell (AC2C) circuits, direct cell to cell (DC2C), cell to pack (C2P), and multicell to multicell (MC2MC) as shown in Table 2 [16,17]. The first group is AC2C function as transference energy between adjacent cells DC2C group having shared voltage equalization circuit for all cells. Meanwhile, DC2C as sharing the voltage equalizer circuit for all cells. For the C2P type transferring the energy between individual cells to the entire string of circuits. The C2P type transfers energy from individual cells to the full string of circuits. In MC2MC, energy was transmitted from multiple cells to multiple cells in a single switching cycle.

Another example of an active equalization at the central part of the DC-DC converter is a modular power converter, which ensures the quick charging and balancing stack of SC [18]. The challenge of this structure is to have a simple structure with a control system that includes a lower bias range of components. The main purpose of this type of circuit is to cut down the cost. However, the integration of SCs in this type produces hundreds of submodules which makes it more complicated. Through this research, the chosen topology review is under cell-to-pack (C2P) categories of active equalizers since the usage of transformer and adjacent cell-to-cell (AC2C) involve switched capacitors.

Table 2
Active equalizers categories

Group	Adjacent cell to cell (AC2C) [19-23]	Direct cell to cell (DC2C) [24-29]	Cell to pack (C2P) [23,30,31]	Multicell to multicell (MC2MC) [16,32-35]
Advantages	Modular design Simply control	Effect of inductor coupling High efficiency	Achieve voltage balance independently Flexible	Faster energy transfer Short time for voltage balancing
Disadvantages	Longer time for voltage balancing	High voltage stress Higher cost	Requires large magnetics	Unable to use for high-frequency applications
Types of groups	Switched capacitor, bidirectional cuk	Flying capacitor, single inductor	Buck-boost, flyback, switch transformer	LC resonant, the circuit with relays
Size	Very small	Large	Very large	Small
Cost	Low	High	High	High
Efficiency (%)	92.9	88	85.7	95

3. Comparison of Equalization Topology

Several sample comparisons between equalization topologies have been summarized in this section. The topology structure and sample of simulation have been undergoing detail through this section.

3.1 Review of Chosen Topology Structure

Figure 2(a) illustrates the one of the topologies structures for the dissipative type reviewed. A dissipative balancing circuit (DBC), also known as a passive balancing circuit (PBC), includes a resistor linked in series or parallel with each cell of the battery, allowing cell voltage to be balanced by dissipating energy such as overvoltage caused by thermal factors. This type of balancing circuit is dependent on the resistor value and the affected current profile due to resistor leakage current, which reduces the efficiency of a supercapacitor as one energy storage system. The probability study that has been undergoing in DBC is divided into two, that is maximum storage energy and zero energy loss. The guideline in designing the supercapacitor is based on output voltage have been specific by three specifications included that available energy, available power, and maximum voltage.

Subsequently, the passive balancing circuit studied in literature is a clamping diode shown in Figure 2(b). Yue *et al.,* [42] stated three clamped methods that focus on load-side voltage balancing methods are clamped snubber, Resistor-Capacitor-Diode (RCD) snubber, and collector-gate voltage (V_{cg}) snubber. Michael *et al.,* [43] suggested a circuit of passive balancing with overcharging protection. The circuits using three-cell Lithium-Ion batteries by additional parallel diode function as dissipation components. Indirectly, the overcapacity of cells can be protected since the ability of circuit dissipation improved. Zarghani *et al.,* [44] described that by create the snubber circuit structure with clamp mode operation that the scheme may employ for any number of switches without altering the real behaviour as one of the distinct components impacting the imbalance voltage, switch-to-ground parasitic capacitance was identified as a significant influence during the transient interval. In addition, by adding a snubber circuit, the parasitic capacitance effect could be decreased and managed to balance the voltage sharing [44]. The creation of a snubber circuit structure with clamp mode operation that the scheme may employ for any number of switches without changing the actual behaviour as one of the distinct components impacting the imbalance voltage, switch-to-ground parasitic capacitance was identified as a significant influence during the transient interval.

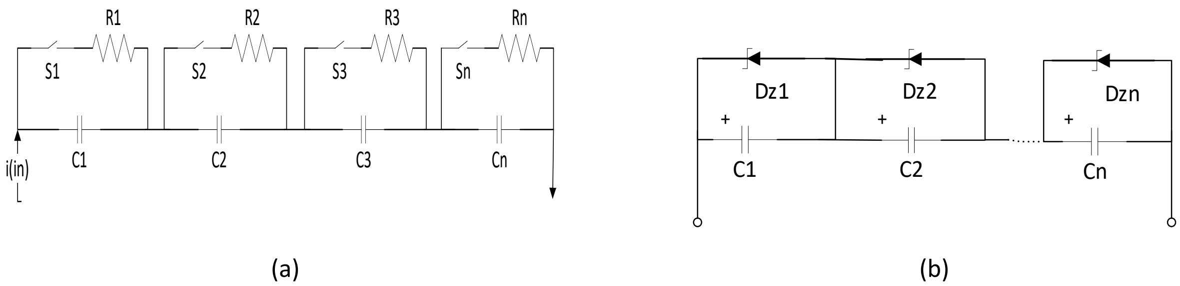
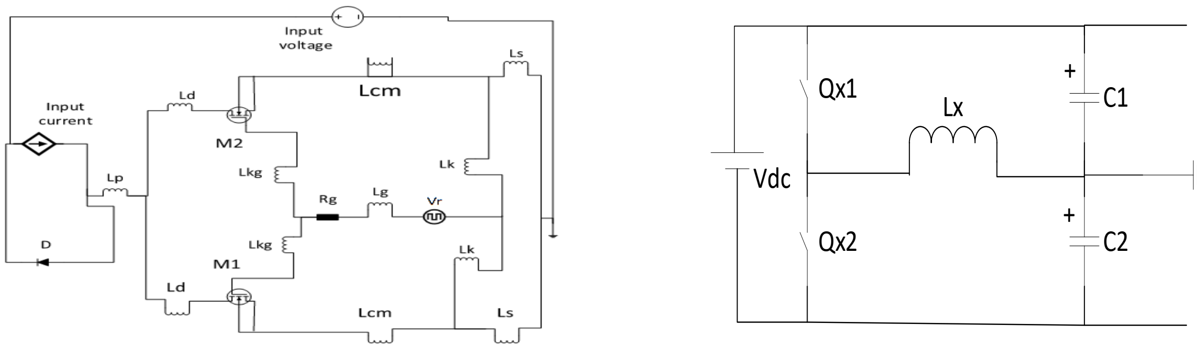


Fig. 2. (a) Dissipative balancing circuit with resistor [36-38], (b) Passive balancing circuit with Zener diode [39-41]

Besides, Figure 3(a) presenting a passive balancing circuit combination of metal-oxide-semiconductor field-effect transistor (MOSFET) and power resistor that are established in [45]. The recommended method uses MOSFET as internal resistance to produce greater balancing current capability. An internal resistance value of MOSFET determined the balancing current of the energy storage system. Meanwhile, Mao *et al.,* [39] suggested balancing passively MOSFETs are being used to investigate the balancing of peak currents between parallel MOSFETs produced by unequal threshold voltages. The change in peak current limit caused by changing one resistance and one inductance per switch without compromising total switching loss. Under various continuous testing conditions, the design criteria include threshold voltage mismatch, current increase time, and imbalanced percentage peak current are clearly shown in [39].

Meanwhile, Figure 3(b) shows one of the structures for non-dissipative balancing circuit that will be reviewed in this paper. The isolated DC-DC converter topologies in active equalizers that have been reviewed in this paper is zero switching voltage (ZVS). There are several models have been stated out about this topology. Farzan and Bossche [50] introduced that for the forward converter, a circuit utilizes a single transistor in a ZVS. The circuit equalizes and is made up of eight cells connected in a series of battery packs. Each battery pack employs a forward converter, whereas the entire battery pack employs a buck converter. To demagnetize the transformer, the application of (ZVS) needed a capacitor in parallel with the switch. Un-Noor *et al.,* [51] proposed ZVS forward converter has a high efficiency, reducing the ringing of diode rectifiers. Meanwhile Un-Noor *et al.,* [51] presented the interleaved ZVS forward converter with voltage double which the scheme reduces the voltage stress and current on the capacitive output filter. A topology that has interleaving allows having equal power in each cell. The voltage doubles the rectifier at the output significantly reducing the number of secondary diodes. There is also some topology ZVS using coupling inductor which been added on the primary side of the transformer using push-pull forward circuit [52].

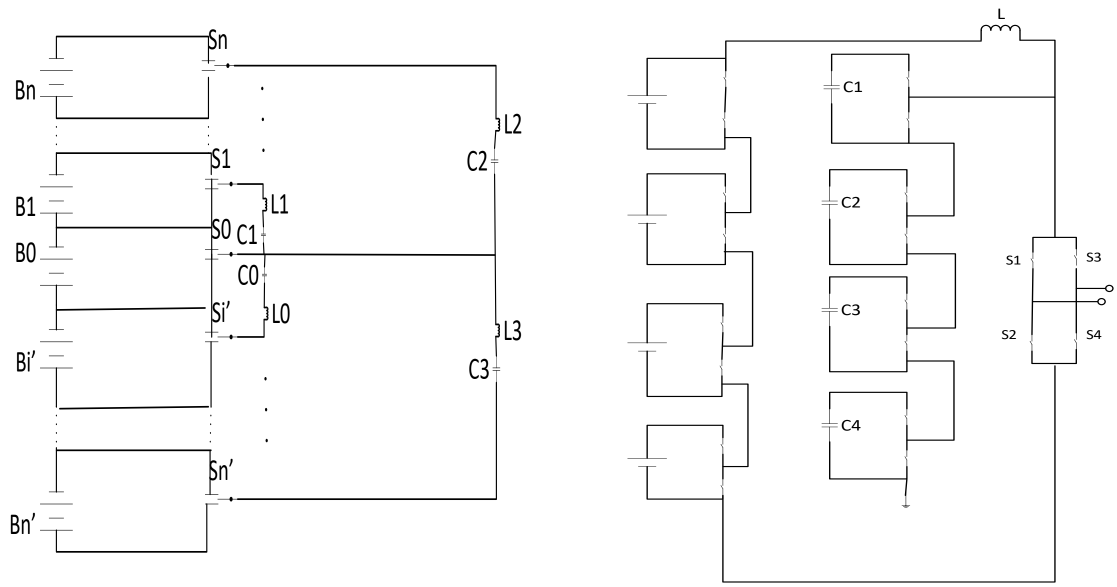


(a) (b)

Fig. 3. (a) Dissipative balancing circuit with MOSFET [7,46], (b) Zero voltage switching (ZVS) [47-49]

The next topology presenting through Figure 4(a) where it is the zero current switching (ZCS) circuit, that reduces switching losses. According to Arab Ansari *et al.,* [53] the ZCS flyback inverter's discontinuous conduction mode (DCM) at the primary switch is detailed, with a simple auxiliary circuit added to the fundamental flyback inverter circuit. During the turn-off procedure, voltage overshoot from the primary switch is controlled, allowing MOSFETs to have lower conduction [54]. The ZCS of switched-capacitor DC-DC converter being introduced to provide soft switching for devices [55-58]. The reason to have DCM because to achieve power efficiency. They are also a ZCS circuit of a current-fed half-bridge converter that intends to clamp excessive voltage spikes across the main switches generated by energy stored in the transformer's leakage inductance. ZCS on and off regulates the rectifier diodes and auxiliary switch [59,60].

Subsequently, Figure 4(b) is the modular cascaded active balancing structures highlighted as major ways for the grid and industry applications. Some examples that have been present in Marzo *et al.,* [65] are Cascaded H-Bridge (CHB) and the Modular Multilevel Converter (MMC). Meanwhile, a power transformer was compared to a three-phase cascaded modular rectifier with a dual active bridge (DAB). The voltage controller for the DAB stage provides balanced dc-link with dc-bus voltage and the proportional-resonant controller used in the inverter stage [63]. Another discovered modular multilevel topology cascade is built on single star bridge cells (SSBC) and single delta bridge cells (SDBC). Six zero-sequence voltage waveforms with variable harmonic content that provide better energy-balancing capabilities are investigated and compared in the SSBC inverter [66]. In Sha *et al.,* [67] presented topology of the first stage consists of a multilevel cascaded H-bridge ac-dc converter, while the second stage consists of modular current-fed dual active bridge dc-dc converters with cascaded H-bridge converter unified control to balance the cascaded H-bridge dc voltages for both charging and discharging modes.



(a) (b)

Fig. 4. (a) Zero current switching (ZCS) [53,55] (b) Modular cascaded active balancing circuit [61-64]

3.2 Review Sample Result of Equalizers Topology

In this part of the research, the verification that has been undergone from chosen topology review is presented. The result is demonstrated based on chosen equalizers that have been shown in the previous section. Various sample result of topology from each equalizer that undergoes the simulation with some discussion and explanation will be summarized in this section.

3.2.1 Sample result of passive equalizers

Through this review, three topologies are recognised and identified: passive balancing circuit in resistor, clamping diode, and MOSFET. Each sample elaborated with some discussion to provide a clear and details understanding for the readers. Supercapacitors are represented as a sequence RC circuit in high-electricity applications, where the ESR symbolizes the voltage drop effect and the equal capacitor denotes the energy storage affects [68]. Following that, Figure 5 illustrates the impact of ESR fluctuations on cell balancing performance. The experiment examined based on Li *et al.,* [69] conducts two stages where first-stage cells are charged with constant current, Ic is 5 A until fully charging and balanced. The discharging process occurs in the second step, where the charging current quickly drops from 5A to 0A. The voltage variation from the three cells is less than 1%, indicating that the voltage drop impact of ESR is ignored in the circuit balancing design. Furthermore, when ESR variation reaches 90% (cell 3 against cell 1), the equivalent variance difference is 0.33 percent, indicating that the influence of ESR variation is minor. The ESR of cells was calculated based on using Eq. (1) [69].

$$ESR_K = \frac{\Delta_{vk}}{i_c} \quad (1)$$

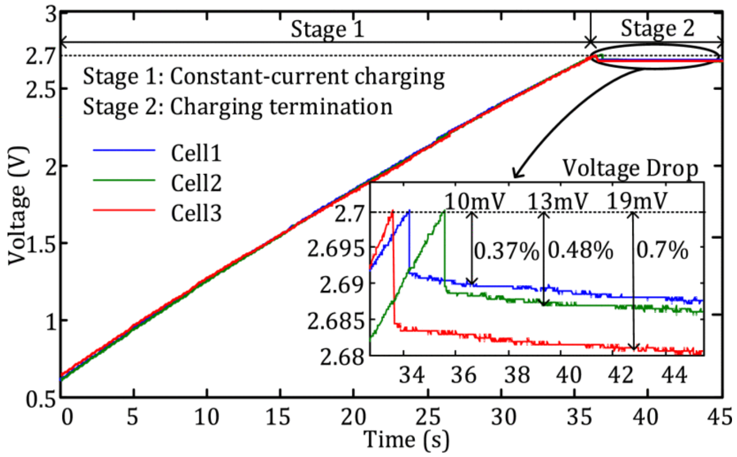
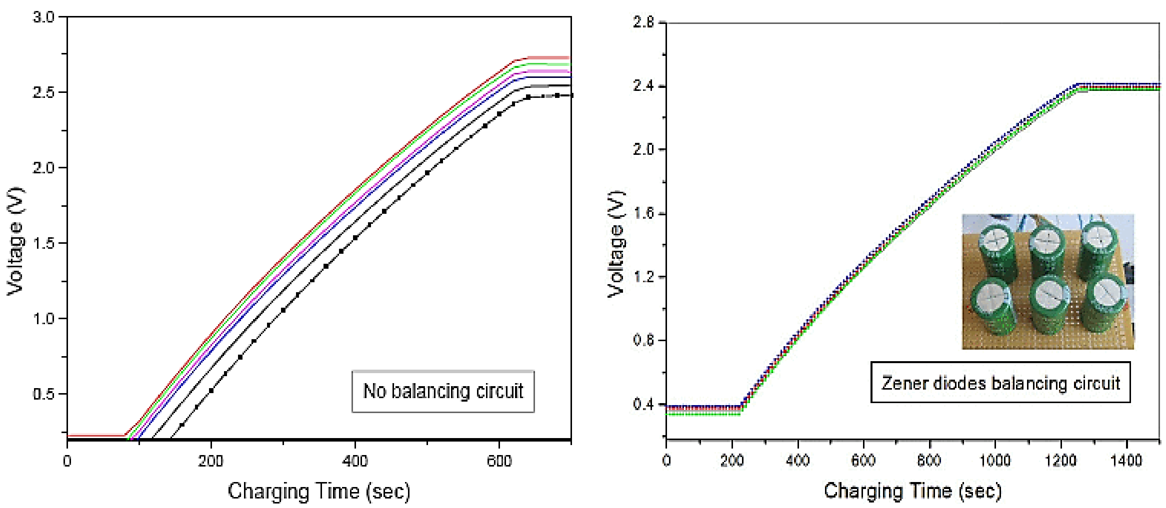


Fig. 5. Switched resistor cell balancing performance [69]

From Ionescu *et al.,* [7], the testing method is used to charge and discharge the supercapacitor module using a constant current. Measurement equipment is also simple: a DC laboratory triple power supply with maximum voltage and current limitation to establish the desired current. The charging current has been lowered to 200 mA for testing the passive balancing circuits based on Zener diodes, as restricted by the maximum diode current. Figure 6(a) shows example data from six channels collected using a Keithley 2700 Integra precision voltmeter fitted supercapacitor module with a 22 F capacitor, revealing varied maximum values when this occurs due to differences in the beginning condition of charging from each capacitor.

Meanwhile, performance after construction of the balancing circuit can be shown in Figure 6(b), which exhibits charge-discharge of capacitors starting charging from a comparable voltage. The clamping voltage limitation based on Zener diode accuracy, as opposed to common diode that can be controlled for commercial use. Accordingly, the reason for the non-identical result measurement happens in this circuit caused by the temperature of Zener voltage as another consideration in the next testing.



(a) (b)

Fig. 6. Zener diode cell balancing performance [7]

The passive balancing method defined to actively track the switching current, one inductor and resistor are used per MOSFET [70]. When the MOSFETs connected in parallel it can boost current capabilities. Since the channel current of a MOSFET unable be measured directly, the drain-source approach must be used before testing by estimating the source current or drain current i_d. Usually, the source current is measured as its grounding reference. As illustrated in Figure 7, the dynamics balancing test uses two brief pulses with switching transients acquired at the initial falling and rising edges at room temperature. The experiment baseline can be observed in Figure 7(a). the balancing effect causes the current imbalance. Alternatively, the impedance of the drive-loop connected to the source, $R_{k,}$ and inductance, L_s designed to get better performance as shown in Figure 7(b). The needed current was achieved in a single switching cycle using a single gate driver that met current balancing requirements.

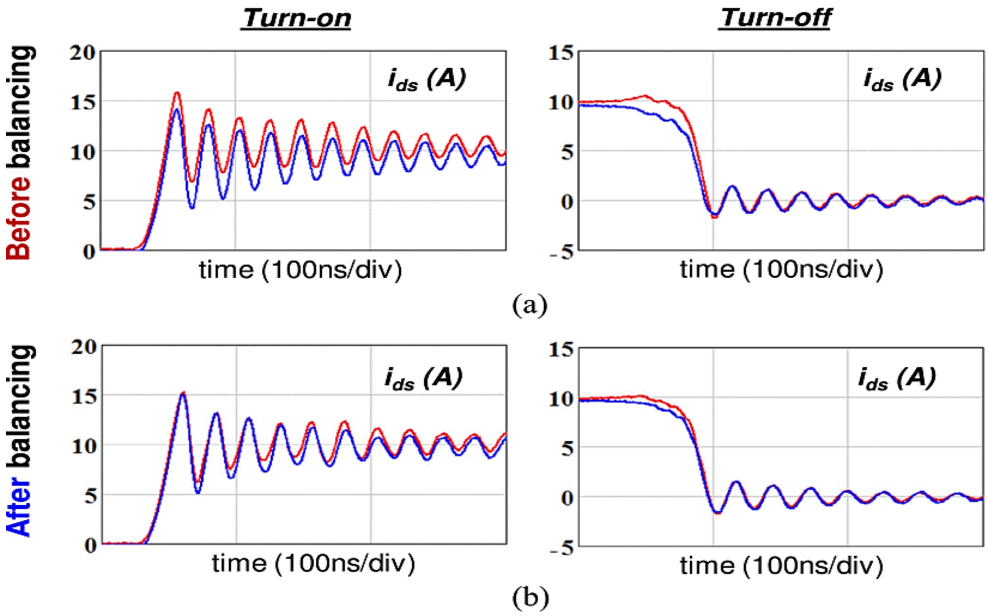


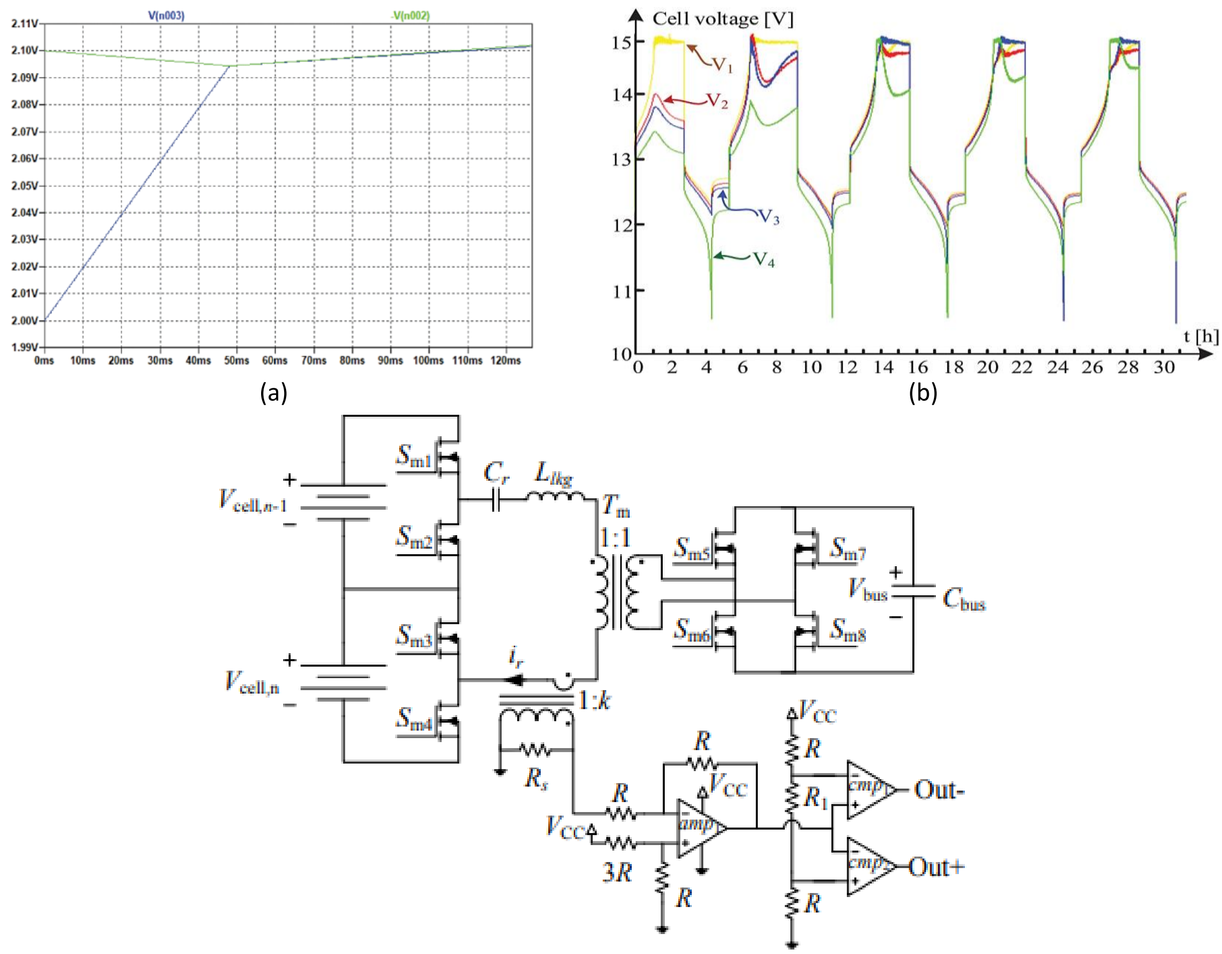
Fig. 7. Zener diode cell balancing performance [70]

3.2.1 Sample result of passive equalizers

Commonly, active equalizers or non-dissipative balancing circuits are based on dc-dc converters. As a result, more power electronics components are required, and circuitry becomes more complicated and expensive. As a result, to reduce the number of passive components by boosting switches with appropriate controls. This paper investigates the sample findings of three active equaliser topologies: zero voltage switching (ZVS), zero current switching (ZCS), and modular cascaded.

The equalization process stated by Arnaudov and Kishkin [28] has started when both supercapacitor cells voltage across cell showing the performance in Figure 8(a) where the green line indicates voltage SC_1 and blue line voltage SC_2. Due to the energy charge received from the entire battery pack, the overall voltage SC2 lowers throughout the equalisation process. At the same time, the main charging converter (MCC) which is a mentioned as constant current source operates at a low charging current, therefore the voltage drop declared above is negligible. The converter stops charging when the voltages across SC_1 and SC_2 reach equivalent values, and the charging process continues with the main charging converter.

For parallel balancing series-connected battery strings, a novel zero current switching design was introduced in Zeltser *et al.,* [71]. The advantage of this topology is that energy is only transmitted when the cells are out of balance. Power losses are decreased indirectly because no current circulates while the system is balanced. The experiment involves five charge-discharge cycles, with the balancing circuit switched off after the first (0-5h). While this balancing circuit is turned off, Cycle 1 is used as a reference. The rest of the cycle's (cycles 2-5) balancing circuit performance is demonstrated. Approximately 1 hour of rest time was provided between cycles to allow cell relaxing processes to complete and the SOC reliable to approximate the results from open-circuit cell voltage. Figure 8(b) depicts the charge-discharge voltage process, in which, once a balancing circuit are turned on, cycle 2 where (6-11h) proceeds to join each other until the last cycle 5 voltage is nearly equally distributed.



(a) (b) (c)

Fig. 8. (a) ZVS balancing performance [28], (b) ZCS balancing performance [71], (c) Implementation of each of the m balancing circuits including the current polarity detection circuitry [71]

Bi *et al.,* [72] shows one example of an active balancing topology for modular cascaded energy storage systems. The fundamental component of the topology consists of a common dc bus voltage loop and an individual current loop for each supercapacitor balancing control submodule. A common voltage loop is utilised to maintain dc bus voltage that is not impacted by SOC balancing management. Meanwhile, SOC information was introduced to provide SOC balancing management. Based on Figure 9 shows the waveforms of the submodule output voltage and current under various conditions whereas in Figure 9(a) the SOC is balanced.

Main surveillance has seen at a duty ratio of each submodule set to be the same, common current ripple happens and the frequency A common voltage loop is utilised to maintain dc bus voltage that is not impacted by SOC balancing management. Meanwhile, SOC information was introduced to provide SOC balancing management.is three times of switching frequency. Meanwhile, Figure 9(b) shows waveforms when SOC is unbalanced under discharge mode. Every submodule operates with a different duty ratio where the highest SOC module is close to 1 and 0.5 is the lowest operating duty cycle. The irregular current ripple in one switch period causes its amplitude becomes larger compared to Figure 9(a). Besides, Figure 9(c) explains that waveforms when SOC is unbalanced under charging mode. The performance is the same as Figure 9(b) but different when the lowest SOC submodule operates at the highest duty ratio and vice versa [72].

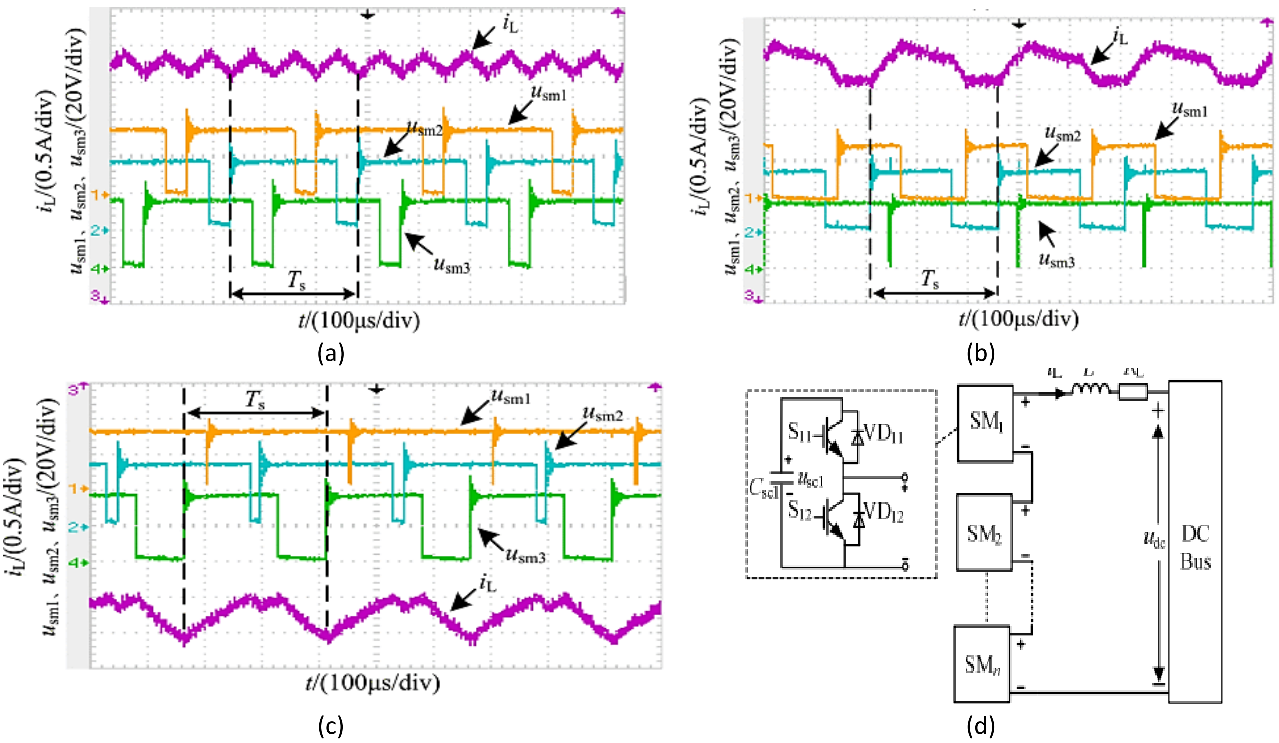


Fig. 9. Modular cascaded balancing performance [72]

Summary from overall reviewing the current researcher's simulation and experiments conducted at both equalizers in describing the performance and reliability of balancing method employed to solve the unbalance circuit with fulfilling the demands. Though, every cell balancing topology vary in its costing, sizing, control complexity, and implementation and fit the application with its benefits and drawbacks.

4. Conclusions

In conclusion, voltage balancing is the main key to prolong the enhanced lifetime and enlarge the available capacity of energy storage system performance. Each operation and verification of reviewed topology of the equalizer is listed briefly as a guideline to improve the energy storage system. Based on several analyses of the topology for voltage balancing in this research, for low power applications, passive equalizers are preferable since it simpler. However, for medium and high-power application active equalizers is the right choice once the system requires additional currents and additional load to avoid energy wasted from the system and get faster equalization time. Thus, passive equalizers have a lower cost with simple topology but lower efficiency.

Additionally, active equalizers offered high efficiency but are quite complicated structure and higher cost. In terms of topologies recorded, most researcher's prefect to establish the works on active equalizers since the great benefit which it transfers energy from higher voltage to lower voltage without consuming power losses that can be implemented in numerous disciplines. Likewise, the choice depends on the applications to ensure the life expectancy of the battery and supercapacitor is not affected with better efficiency.

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