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A Hybrid CMOS Digital-to-Analogue Converters Design for High Resolution SAR ADC

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ABSTRACT

The paper describes the design and implementation of a 14-bit differential Digital-to-Analogue Converter (DAC) based on the Silterra 0.18µm Complementary Metal-Oxide-Semiconductor (CMOS) process to be established in a Successive Approximation Register (SAR) Analogue-to-Digital Converter (ADC) for the purpose of high-resolution, high accuracy and low power applications. The proposed differential DAC aims to eliminate the issue of stringent matching requirements imposed on high-resolution DACs while leveraging both linearity performance and power consumption parameters at a balanced point. The overall differential circuit consists of two parallel single-ended DACs that utilize a 4-bit Capacitor DAC (CDAC) and 10-bit Resistor DAC (RDAC) on each end, thereby establishing a hybrid-based architecture. Furthermore, the authors illustrate the proposed switching procedures applied to the sub-DAC circuits to ensure a low-power design is established. The new method effectiveness evaluation is confirmed by detailed transient simulations implemented on the DAC where the circuit performs the required conversions at a maximum conversion frequency of 2.5 MS/s with a peak power consumption of 0.1496mW for the standard voltage supply of 2.1V. Meanwhile, the schematic and post-layout simulations performed on the DAC registers peak DNL errors of -0.1612 and -0.8272, respectively. New research results depict performance improvements in terms of resolution and power consumption which facilitates the DAC implementation in contemporary electronic devices such as microcontroller peripherals and audio amplification devices. The overall deigned circuit is capable of achieving the desired 14-bit digital-to-analogue conversions under the CMOS 0.18µm technology, proving the DAC's high-resolution efficacy.

1. Introduction

The continuous advancement in the field of Complementary Metal-Oxide-Semiconductor (CMOS) technology has led to the increased demand of low power and area efficient Analogue-to-Digital Converters (ADC) for its application within various highly integrated instruments as well as other

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wireless or portable electronic devices, which are taken from a previous study by Xin *et al.,* [1]. Based on another study by Ng [2], it is also an important feature in modern consumer electronics applications as its function as a mixed-signal circuit is crucial in converting a continuous analogue input signal into a discrete digital output, which in turn would allow the digitally encoded devices to process the anunalogue signals. With various ADC architectures currently being developed in the modern world, the review paper by Wei *et al.,* [3] cites the key area of focus for circuit designers as the implementation of a design that achieves an optimum balance between the trade-offs of speed, power, and resolution.

In this paper, the main research contribution is focused on the design of the DAC component which aims to achieve performance improvements in terms of resolution, conversion linearity and power consumption. The overall scheme of the DAC is created with pure intentions of achieving full compatibility with its corresponding ADC design. Therefore, the design and implementation of the DAC must be carried out effectively as it poses as a crucial circuitry block of the ADC.

The proposed hybrid capacitor array and resistor string architecture that is implemented in a segmented manner enables the DAC resolution to be enhanced via the combination of different types of sub-DACs together. The data taken from the previous study by Xingyuan *et al.,* [4] have shown that these methods are widely implemented in high-resolution SAR ADCs of 12 bits or greater. These types of circuits are also highly sought after in line with the advancement of wireless sensor networks and very-large-scale integration (VLSI) applications, which correlates with the reviews performed by Chen *et al.,* [5], Gaddam *et al.,* [6] and Fan [7]. Additionally, the work performed by Ma *et al.,* [8] has revealed that the implementation of this hybrid architecture has the unique advantage of allowing designers to introduce different types of methods to optimize each sub-DAC based on their individual design requirements and other uncorrelated process parameters, thereby enabling the overall performance of the full DAC circuit to be adequately enhanced. Furthermore, the work carried out by Kim *et al.,* [9] explained that the separation of the resolution bits across two distinct components is mutually beneficial to both sub-DACs as it helps to relax the matching requirement of the 10-bit RDAC (only used for the 10 LSBs) by a factor of 2^4, whereas it reduces the total unit capacitors required for the 4-bit CDAC (only used for the 4 MSBs) by a factor of 2^{10}. This would enable the overall die area to be substantially reduced as the number of DAC components tend to increase exponentially with resolution without the presence of segmented circuit arrays.

Moreover, the work by Ma *et al.,* [8] further elaborated how the expansion in the number of components within the DAC often results in stringent matching requirements which affects the conversion linearity of the DAC. Most uncalibrated capacitive DAC designs also impose similarly strict linearity requirements which require the circuitry devices (e.g., unit capacitors) to be set at larger sizes in order to offset component mismatch and achieve the desired linearity performance. This in turn creates a ripple effect where higher power consumptions are incurred by these circuits due to the larger dimensions required for it to overcome the said mismatch issues and achieve accurate matching and linearity. This concept is further justified by Jung *et al.,* [10].

In the light of these design issues, the novel hybrid DAC proposed in this paper aims to bridge the research gap through the implementation of a design that has the objectives of achieving high resolution, optimum conversion linearity and low power consumption. The proposed circuit utilizes a combination of a 4-bit binary-weighted CDAC and a 10-bit that is subdivided into two individual parallel 5-bit strings. With the applicability of the aggregate 14-bit hybrid design, the overall architecture aims to overcome the limitations of low-resolution circuits while simultaneously meeting the increased demand for high-resolution DACs with superior conversion linearity and accuracy in modern-day electronic applications, as described by Savitha and Reddy [11].

Furthermore, the work by Zhang *et al.,* [12] has illustrated that the hybrid design is able to reduce the number of unity elements within the DAC and improving device matching which allows the circuit to exhibit substantial linearity. The attainment of superior conversion linearity via the binary-weighted design would further ensure that the unit capacitor sizes (and thus unit capacitance) in the CDAC can be reduced substantially, which in turn contributes to a lower power consumption by the DAC circuit. Generally, the development of the proposed hybrid architecture strives to acquire an optimal setting that leverages the trade-offs between the linearity performance and power consumption parameters at a balanced point, which is a concept that is also supported by Saberi *et al.,* [13]. The final design trait undertaken to generate minimum power consumption within the DAC architecture is the employment of the switching methods in both the sub-DAC circuits to ensure that only the required switches are activated for each of their respective conversion processes. In terms of research contribution, the integration of the proposed high-resolution DACs in microcontroller peripherals would improve the precision of the output analogue voltage as it is divided over a greater number of digital bits, thereby making the voltage step for the converted bits more discrete in value. This concept also holds true in audio amplification devices where a well-designed DAC would enable a high-resolution of the output analogue audio as there are more digital bits are available for conversion. Furthermore, a high precision DAC able to perform accurate conversions and yield more precise output signals with minimal errors or glitches.

2. Methodology

The proposed hybrid Resistor-Capacitor DAC is implemented using the Virtuoso Cadence Tools which incorporates of several fundamental circuit blocks, namely the 4-bit Multiplexer (MUX 4), 4-bit binary weighted Capacitor DAC (CDAC), 10-bit Multiplexer (MUX 10), and 10-bit binary weighted Resistor string DAC (RDAC). These circuitry blocks work in unison to constitute the 14-bit digital-to-analogue conversion functionality of the DAC.

2.1 Block Diagram

The block diagram in Figure 1 illustrates the single-ended DAC architecture that comprises all the requisite components of the proposed hybrid circuit. Initially, the 14-bit digital bits sent from the output of the ADC is used as an input simulation that is received by the 10-bit Multiplexer (MUX 10) and 4-bit Multiplexer (MUX 4). These multiplexers process and control the corresponding input signals that are delivered to the 10-bit Resistor DAC (RDAC) and 4-bit Capacitor DAC (CDAC). The digital-to-analogue conversion process is subsequently performed by both DACs where the first 4 Most Significant Bits (MSBs) are resolved by the 4-bit CDAC, while the remaining 10 Least Significant Bits (LSBs) are converted by the 10-bit RDAC. Upon completion of the conversion process, the output signal produced by the 10-bit RDAC is initially directed into the 4-bit CDAC before being complied with the CDAC output to generate the finalized analogue signal of the DAC.

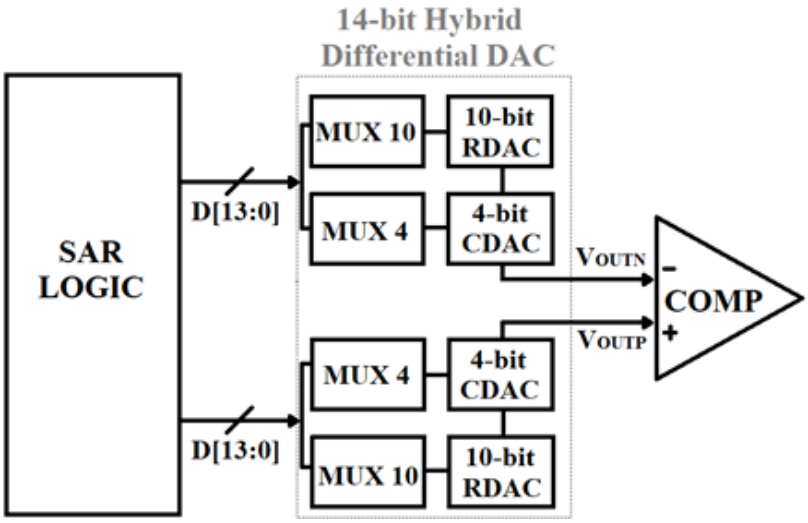

Fig. 1. Block Diagram of the 14-bit single-ended hybrid DAC

2.2 4-bit Multiplexer (MUX4)

The 4-bit Multiplexer (MUX4) receives the 4 MSBs from the ADC and processes these bits to deliver the required output bits to the Capacitor DAC (CDAC) as well as the govern the operation of the circuit. The schematic diagram of the MUX4 is shown in Figure 2, which comprises of four identical logic gate arrays with input ports IN<0:3> that receive the four digital bits from the ADC, the PHI1D ports that are connected to each multiplexer, and another eight output ports classified as OUT<0:3> and OUTB<0:3> that are connected in pairs to each of the multiplexers. During the sample phase, the output signal from OUT<0:3> yields a contrary bit to that of OUTB<0:3> due to the inversion process that takes place between these two ports after the PHI1D switch is opened. These pairs of ports are the only contact point between the MUX4 and CDAC, thereby giving them complete control over the signals that enter the CDAC which influences the output performance of the circuit.

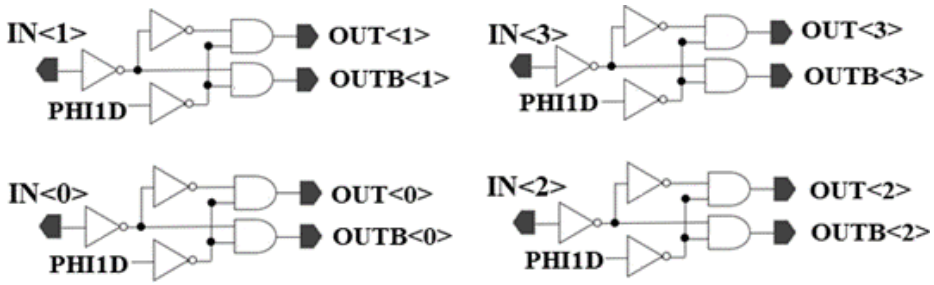

Fig. 2. Schematic Diagram of the 4-bit multiplexer (MUX4)

2.3 4-bit Capacitor DAC (CDAC)

The main body of the 4-bit CDAC constitutes five arrays of binary-weighted capacitors where the first 4 sets are arranged in decreasing binary order (C_3, C_2, C_1, C_0) from left to right as shown in Figure 3. These capacitors and their respective switches receive and convert the 4 MSBs (delivered from the MUX4) into their respective analogue voltages. On the other hand, the dummy capacitor (CD) array integrates 20 symmetrically arranged dummy units that protect the outer layers of the actual capacitors from being potentially damaged or removed during the fabrication process, all of which could lead to severe degradation in capacitor performance.

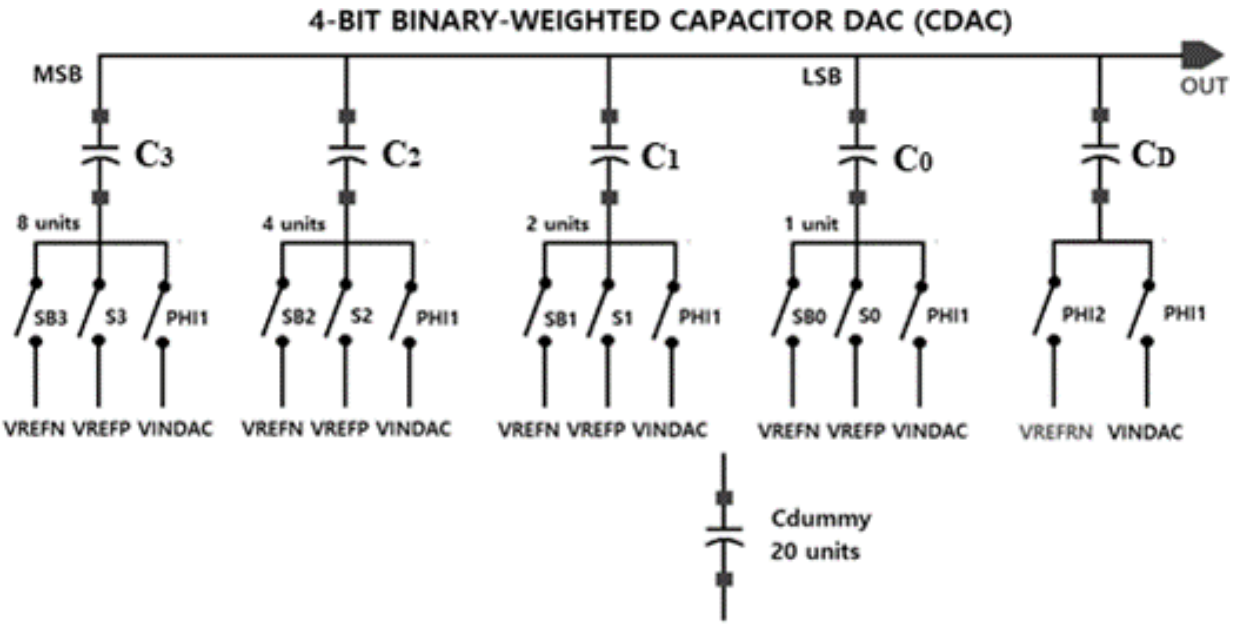

Fig. 3. Schematic Diagram of the 4-bit Capacitor DAC (CDAC)

The binary-weighted architecture is implemented in the CDAC as it exhibits better conversion linearity than that of the split-capacitor array, making it a more common application in low-speed and high-resolution DACs where strong linearity performance is required. This principle is vindicated by Liu *et al.,* [14] through their work. The dimensions of each CDAC unit capacitor are also an important design parameter that determines the DAC linearity. As theoretically explained by Sun *et al.,* [15], the smallest admissible unit capacitance that can be provided for the CDAC for a certain linearity requirement is set by the capacitor mismatch, which in turn specifies the minimum area of each unit capacitor. In the proposed design, the smallest allowable unit capacitance required to achieve proper linearity is 10.0437pF, whereas the minimum requisite dimensions of each unit capacitor are 100µm×100µm.

Each binary capacitor array has an individual set of Transmission Gate (TG) switches connected to their respective supply voltages, which include the Positive Reference Voltage (V_{REFP}), Negative Reference Voltage (V_{REFN}) and DAC Input Voltage (V_{INDAC}). These switches correlate to the independent operational process of the CDAC that is subdivided into the reset cycle and sample cycle. During the reset cycle, the PHI1 and SB <0:3> switches are turned off which enables the CDAC to be connected to the V_{REFN} port and all capacitors to subsequently discharge themselves. Meanwhile, the PHI1 switches are opened during the sample cycle while the remaining S and SB switches are turned on or off based on the digital input bits received from the MUX4. A digital 1 or HIGH input bit would close the S <0:3> switches which connects the CDAC to the V_{REFP} port. Conversely, the SB<0:3> switches are triggered during a digital 0 or LOW input state, which in turns enables the CDAC and V_{REFN} port to be directly connected.

The switching cycles that occur during the independent operation of the CDAC sets up the circuit for its subsequent operation of converting the 4 digital MSBs into their respective analogue voltages. Generally, the switching method implemented on the CDAC ensures that only the necessary switches are activated during the bit retrieval and conversion process of the CDAC operational phase, while the inessential switches are left open. Therefore, the CDAC is able to avoid excessive power consumption which helps the circuit to achieve better energy efficiency.

2.4 10-bit Multiplexer (MUX10)

The 10-bit Multiplexer (MUX10) receives the 10 digital LSBs from the ADC and processes these bits to deliver an accurate output signal through the TG switches that are subsequently delivered to the RDAC. The schematic diagram of the MUX10 is shown in Figure 4, where the 10 digital bits sent from the ADC are received by the I<9:0> input ports. Meanwhile, the main body of the MUX10 consists of 33 identical logic gate arrays with SM<0:32> labelled output ports that control the main string switches within the RDAC, along with an additional 32 identical logic gate arrays classified as SL<0:31> in their output ports which control the sub string switches of the RDAC. The SM and SL ports are the eventual output of a series of logic gates connected in the form of a combinational logic circuit which serves as the only contact point between the MUX10 and RDAC, thereby enabling them to deliver the desired output signal from the MUX10 that governs the operations of the RDAC.

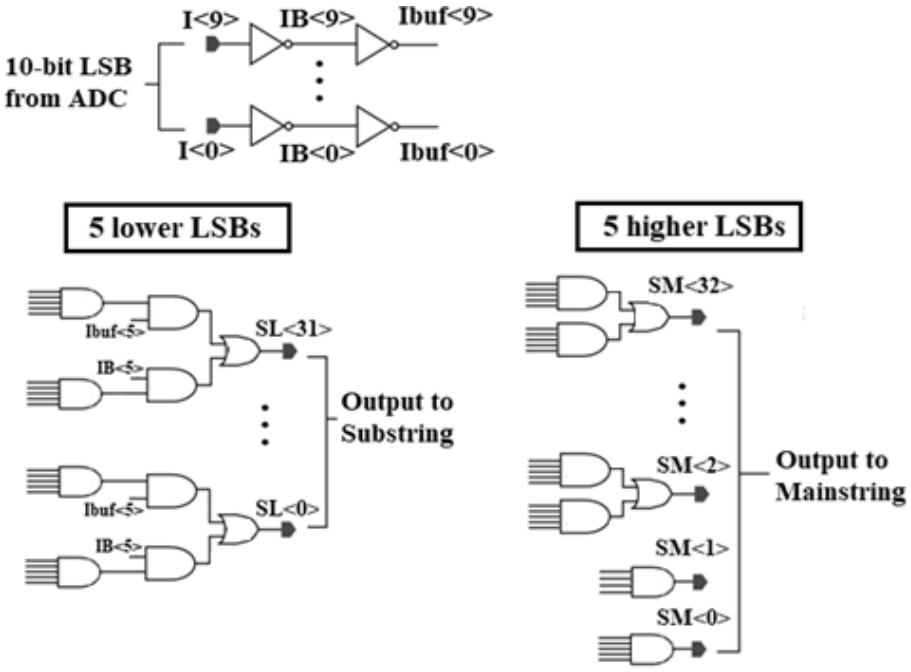

Fig. 4. Schematic Diagram of the 10-bit multiplexer (MUX10)

2.5 10-bit Resistor DAC (RDAC)

The RDAC circuit in Figure 5 comprises a segmented resistor string DAC that is divided into a 5-bit main string (SM) and 5-bit sub string (SL) DAC. The TG switches are categorized in a similar manner to that of the MUX10 output ports where those in the main string are labelled as SM<0:32> while SL<0:31> are used to designate the switches in the sub string. The control exerted on these switches by the output signals sent from the MUX10 ports ensures that only the required switches are closed and connected to their respective resistors for each specific input code while the remaining unused switches are kept open. This operation concept outlines the switching method implemented in the RDAC which are part of the efforts to reduce the power consumptions within the RDAC and across the whole DAC in general. Table 1 depicts this switching method where only a maximum of three switches are triggered for each input code conversion. The switching procedure starts at the null code through the activation of the SM<0>, SM<1> and SL<0> switches, with the sequence moving in ascending order along the sub string for each subsequent digital code until it arrives at SL<31>. Following this, the first two stimulated switches are transferred over to SM<1> and SM<2> while the

sub string count moves in descending order from SL<31> back to SL<0> in correlation with the input code ascension. This switching process is repeated until the sequence reaches the final input code count and the last of the closed switches combination at SM<31>, SM<32> and SL<0>.

Table 1
Closed switches for each input code in the RDAC switching method

Input Code	Closed Switches
00 0000 0000	SM<0>, SM<1> and SL<0>
00 0000 0001	SM<0>, SM<1> and SL<1>
00 0000 0010	SM<0>, SM<1> and SL<2>
…	…
00 0001 1110	SM<0>, SM<1> and SL<30>
00 0001 1111	SM<0>, SM<1> and SL<31>
00 0010 0000	SM<1>, SM<2> and SL<31>
00 0010 0001	SM<1>, SM<2> and SL<30>
…	…
11 1111 1110	SM<31>, SM<32> and SL<1>
11 1111 1111	SM<31>, SM<32> and SL<0>

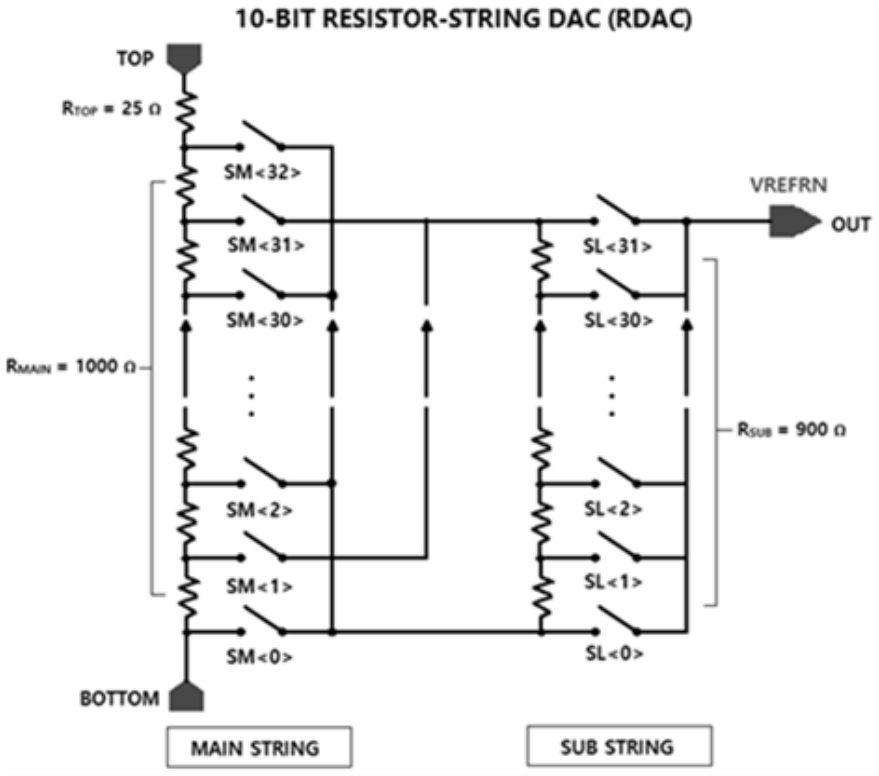

Fig. 5. Schematic Diagram of the 10-bit Resistor DAC (RDAC)

The implementation of this switching technique ensures that the switches and resistors work in collaboration to convert the digital codes sent from the MUX10 into a 10-bit equivalent analogue voltage with minimum power expenditures. Following this, the output voltage is sent through the VREFRN output port of the RDAC to the corresponding V_{REFRN} port connected to the CD switches in the CDAC, where this voltage is compiled together with the 4-bit analogue voltage of the CDAC to generate the finalized 14-bit output voltage that is transmitted from the output port of the CDAC (OUT).

2.6 Top-Level Single-Ended DAC

The top level singled-ended DAC schematic shown in Figure 6 is constituted of all the fundamental circuit blocks which include the MUX4, MUX10, CDAC and RDAC. Each block contains the schematic diagram of their respective circuits with all the major input and output ports attached externally to enable more direct connections to be established between interactive blocks, such as the MUX4 and CDAC as well as the MUX10 and RDAC.

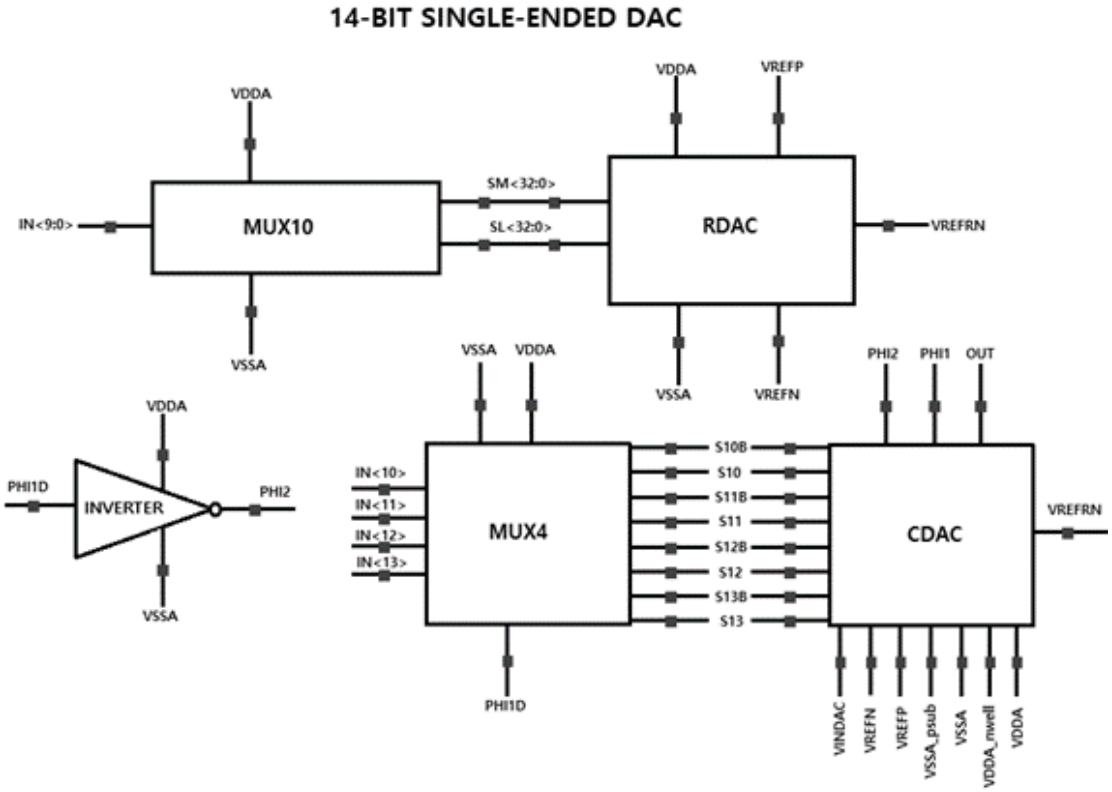

Fig. 6. Schematic diagram of the 14-bit single-ended DAC at the top level

2.7 Top-Level Differential DAC

The top-level differential DAC is essentially a compilation of two identical single-ended DACs arranged in parallel. The reversal of the negative voltage reference (V_{REFN}) and positive voltage reference (V_{REFP}) ports in the second DAC would yield an output voltage that is symmetrically inverted to that of the initial block. The generation of these two individual single-ended output voltages, namely the N-voltage Output (V_{OUTN}) and P-voltage Output (V_{OUTP}) constitute the differential output voltage (V_{DIFF}) of the entire differential DAC that is calculated by taking the absolute difference between V_{OUTN} and V_{OUTP}.

2.8 Layout Design

The layout design of the differential DAC is drawn in the enhanced Virtuoso Layout Suite of the Cadence Tool which correlates to the subcomponents within the schematic diagram of the differential DAC. The layout design of the top-level differential DAC shown in Figure 7 incorporates two identical single-ended DAC layouts, whereby the bottom DAC is flipped 180^o horizontally to constitute a mirror image of the top DAC. In each single-ended circuit, the CDAC is used to form the

base of the layout as it has the largest area among all the subcomponents. The placement of the MUX4 directly above the CDAC enables a direct wiring connection to be established between the MUX4 output ports and the input ports of the TG switches within the CDAC. Similarly, the RDAC and MUX10 circuits are placed in adjacent with their corresponding ports aligned with one another to ensure that a minimum-length wiring connection is routed between the two circuits. The overall configuration is designed in a manner that generates minimum parasitic features to be extracted from the layout blocks, which reduces the degradation effect of these parasites on the DAC performance in terms of voltage accuracy and Differential Non-Linearity (DNL) errors.

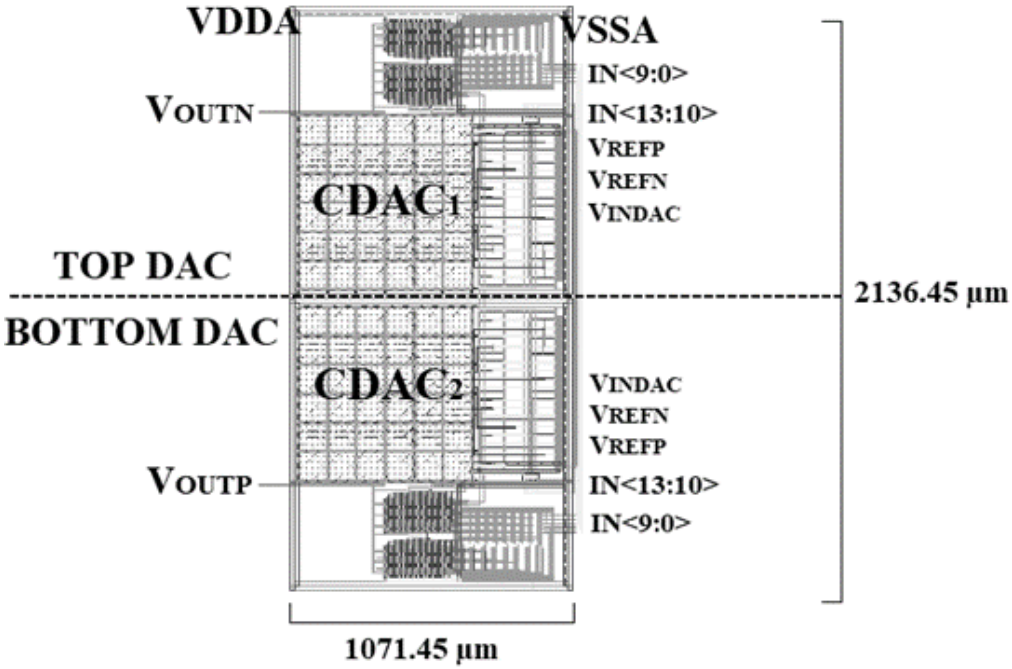

Fig. 7. Layout design of the top-level differential DAC

3. Results

The detailed transient simulations for the digital-to-analogue conversion process of the 14-bit differential DAC are performed using the Virtuoso Analogue Design Environment L (ADE L) tool in the Cadence software. The ADE L simulation tool enables the functionality and performance of the DAC to be assessed in terms of its DNL errors, resolution and power consumption. The simulations are performed under typical circuitry conditions which incorporate a higher voltage analogue supply rail (V_{DDA}) of 2.1V and an operating temperature of 27^{o}C (room temperature).

The simulation of the differential DAC induces two distinct digital-to-analogue conversion processes occurring simultaneously due to the incorporation of two single-ended components. This conversion process that takes place over a range of increasing digital codes would create an output differential voltage (V_{DIFF}) graph that resembles a staircase function, whereby the magnitude of each voltage step is equal to an LSB step-sized voltage output (V_{LSB}). Since 2.1V voltage is used in each single-ended DAC, the full-scale voltage of the differential DAC is double that value. Therefore, the magnitude of a single VLSB step for a 14-bit DAC can be calculated using the formula shown in Eq. (1).

$$V_{LSB} = \frac{4.2\,V}{2^{14}} \approx 256\ \mu V \tag{1}$$

Furthermore, the voltage accuracy of the simulated VDIFF output is assessed via the Differential Non-Linearity (DNL) parameter which essentially measures the discrepancy between the ideal and actual VDIFF output. Therefore, a low DNL is indicative of an accurate output voltage of the DAC and vice versa. Should the VDIFF output face any distortions due to mismatch errors or non-linearities, an irregular VLSB step value would be recorded which significantly increases the DNL value. Generally, the absolute value of the DNL represents the number of missing voltage steps or codes in the VDIFF output, which is the main reason why this parametric value must be kept within a range of +/- 1.0 to avoid any codes from being missing in the output differential voltage.

3.1 Schematic Level Simulation

Upon prior trial and simulation of the digital-to-analogue conversion processes of all 16384 (2^{14}) input codes, a few 'critical codes' have been selected to undergo detailed scrutiny in this paper where higher DNL errors were detected due to certain abnormalities in the conversion process. An example of such critical codes is the mid-code transition ranging from 01 1111 1111 1111_2 (8191) to 10 0000 0000 0000_2 (8192) where all the resistors and capacitors undergo simultaneous transitions. The simulation process is performed across the 6 input codes from 8189-8194 that include the mid code (8192) which enables the main differences between the V_{LSB} step of a regular code conversion and that of the mid-code transition to be clearly discerned. Figure 8 shows the transient simulation result of the V_{DIFF} at this mid-code transition. The V_{DIFF} graph descends relatively smoothly resembling the staircase function, but a temporary jitter occurs at the transitional code where the plot briefly deviates from the ideal staircase function before recovering to a reasonably stable value. This glitch is mainly due to the mismatch properties between the different weighted capacitors as the mid-code transition involves a shift of the active HIGH status from C4 to C8 in the CDAC. This would lead to the V_{DIFF} at the exact transitional code having an unusual step size of 297.7 µV and a maximum DNL value of -0.1612 LSB at the same transition point, as shown in Figure 9.

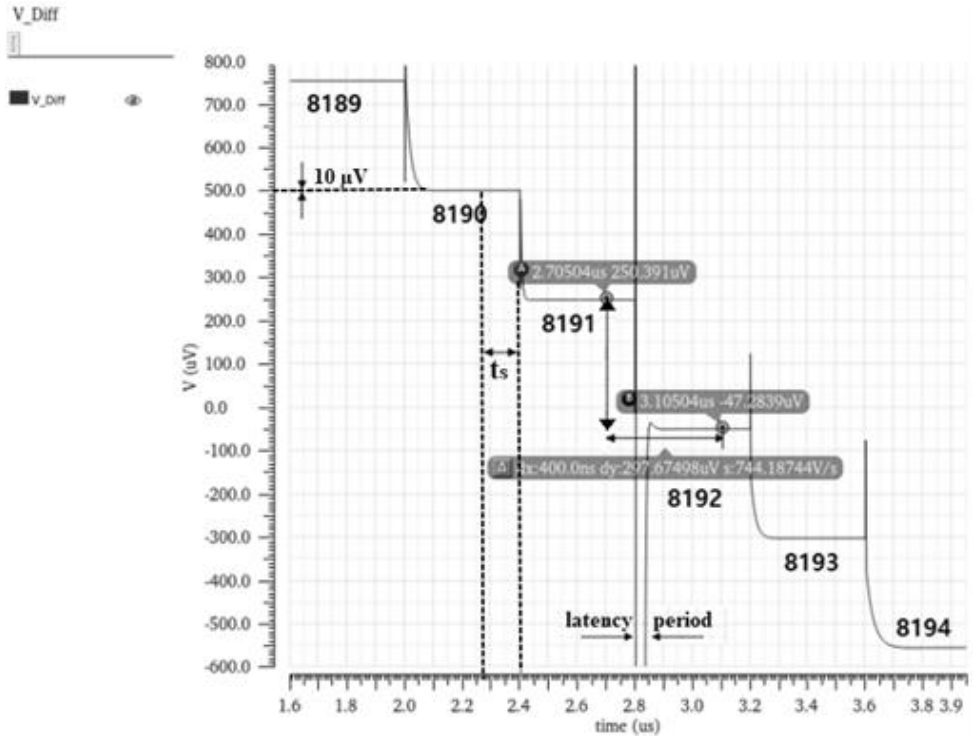

Fig. 8. Output differential voltage (V_{DIFF}) of the differential DAC at the mid-code transition (Schematic Level)

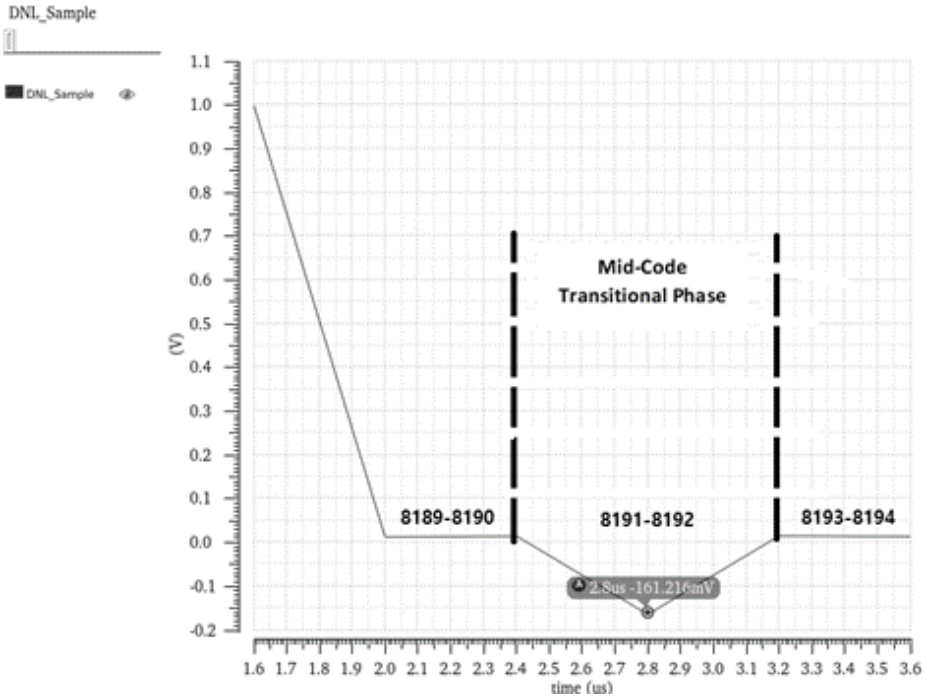

Fig. 9. DNL errors of the differential DAC at the mid-code transition (Schematic Level)

The simulation process is subsequently repeated for another two sets of critical codes. The first set comprises the input codes ranging from 4092-4097 to observe the quarter-code transition from 00 1111 1111 1111_2 (4095) to 01 0000 0000 0000_2 (4096). In this instance, the C4 capacitor switches its status to HIGH while all the lower bit capacitors and resistors after it are changed to a LOW status. Again, this transition process involves a switch of HIGH status between distinct binary capacitors (C2 and C4) of different matching properties, which would inevitably lead to an offset in the ideal step size and contribute to a slightly higher DNL value.

Meanwhile, the second set involves the shortlisting of codes from 1021-1026 as it covers the transitional codes from the MSB of the RDAC at 00 0011 1111 1111_2 (1023) to the LSB of the CDAC at 00 0100 0000 0000_2 (1024). Under these conditions, the main and sub string resistors of the RDAC simultaneously change their statuses to LOW, which leaves the LSB capacitor in the CDAC (C1) as the sole component to switch to a HIGH status. Therefore, the loading effect that exists between the two resistor strings along with the inherent mismatch properties between the different structured RDAC and CDAC would inevitably lead to a less-than-ideal conversion process across the transitional code.

Upon simulating these two sets of input codes under the same settings as those of the mid-code transition, the simulation results reveal a similar performance level of the DAC in regard to the V_{DIFF}, DNL errors and settling time. These performance data are summarized in Table 2. As a voltage settling period of 400 nanoseconds (ns) is achieved by the DAC across all the critical input codes, the maximum conversion frequency acquired by this circuit is deduced at 2.5 MS/s (1/400ns).

Table 2
DAC performance at the critical input codes (Schematic level simulation)

Parameter	Mid-Code	Quarter-Code	RDAC-CDAC
V_{DIFF} at critical code (µV)	297.7	297.4	297.6
DNL (LSB)	-0.1612	-0.1601	-0.1610
Voltage settling time (ns)	400	400	400

3.2 Parasitic Extraction

The parasitic extraction (PEX) is carried out using the calibre parasitic extraction tool that performs extraction and interconnection of the layout parasites hierarchically. The complete PEX process enables the layout netlist to be extracted which contains all the parasitic resistances and capacitances that are existent within the differential DAC. The layout netlist poses as a significant inclusion in the post-layout simulation which serves to illustrate the effects of the parasitic features on the overall performance of the DAC.

3.3 Post-Layout Simulation

The post-layout simulation carried out in similar fashion to that of the schematic level simulation but the additional inclusion of the layout netlist file into setup environment to allow the simulation to be implemented with the inclusion of the layout parasites. The first of these simulation processes once again takes place at the mid-code transition of the differential DAC. The simulation result is shown in Figure 10, where the VDIFF graph assumes a similar staircase function to that of the schematic level simulation, but with a more significant jitter in the transitional steps. The effect is more apparent at the mid code change, where an initial distortion in the output voltage causes the step size to be unusually higher at 411.8 µV and a resulting maximum DNL value of -0.6063 at the same transition point (shown in Figure 11). Therefore, the inclusion of the layout parasites within the simulation process coupled with the mismatch properties between the different weighted capacitors has adverse effects on the DAC performance in terms of the VDIFF accuracy distortion and significantly higher DNL levels.

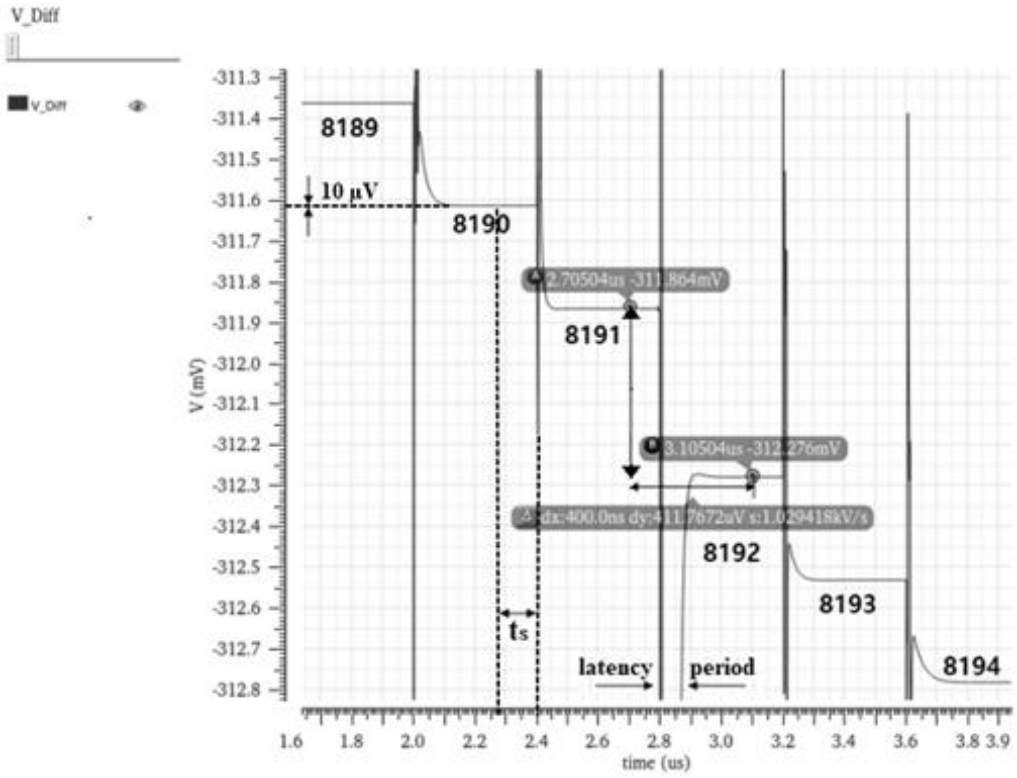

Fig. 10. Output differential voltage (V_{DIFF}) of the differential DAC at the mid-code transition (Post-Layout)

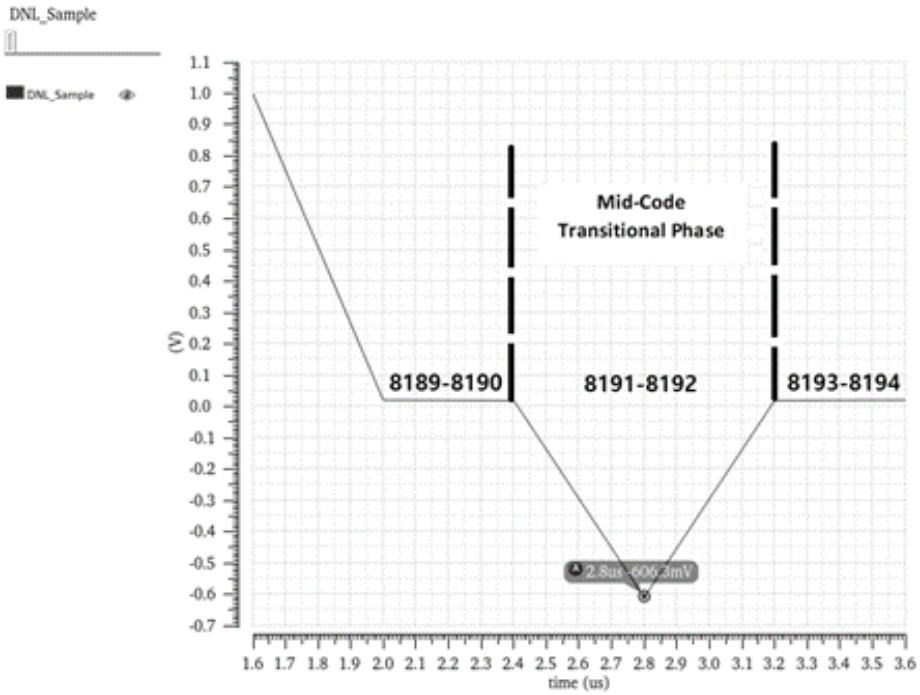

Fig. 11. DNL errors of the differential DAC at the mid-code transition (Post-Layout)

In regards to power, the output current trace for the entire mid-code conversion process is shown in Figure 12, with the average current flow within the circuit being enlisted in the top right of the figure. The average current magnitude of 71.25µA and VDDA of 2.1V induces a maximum power consumption of 0.1496mW by the differential DAC across the mid-code conversion process.

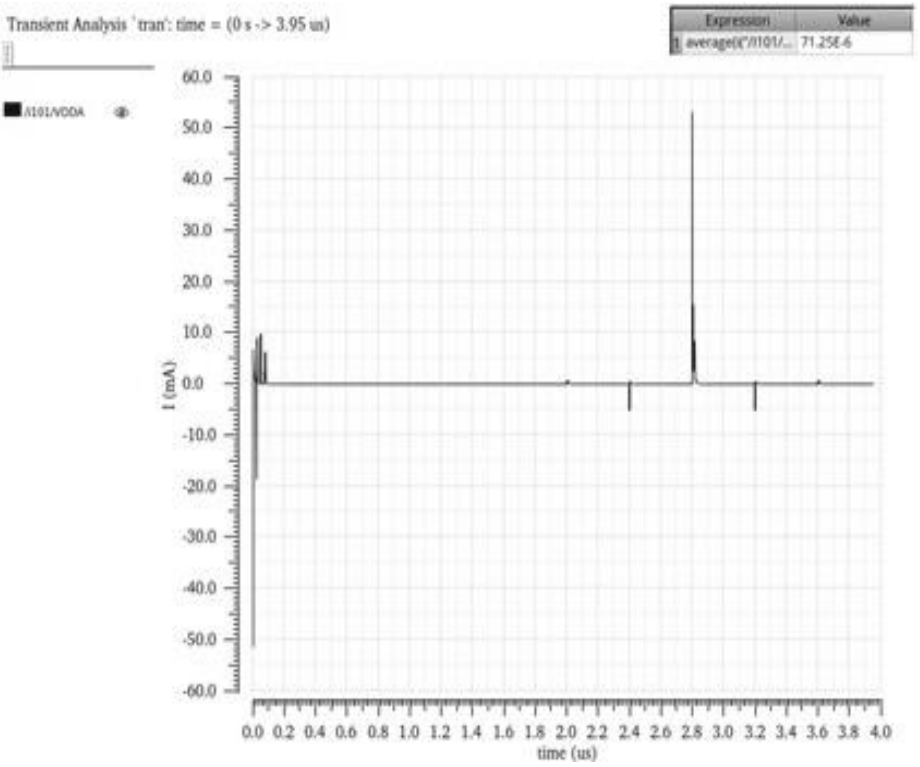

Fig. 12. Output current trace and average current consumption at mid-code transition (Post-Layout)

Subsequently, the post-layout simulation process is repeated for the input code sets that encapsulate the quarter-code and RDAC-CDAC transitions. Based on the simulation results in Table 3, it can be deduced that the layout parasites have negative implications on the DAC performance as all the critical code transitions register significantly higher VDIFF and DNL errors in comparison to their schematic level counterparts. Nevertheless, the DNL levels are still within the requisite +/-1.0 range, meaning no missing codes are present in the output voltage which deems the simulation results acceptable. Conversely, the alterations in the post-layout analysis had no implications on the voltage settling periods of all the critical codes, thereby retaining the conversion frequency at a maximum value of 2.5MS/s throughout the entire DAC simulation process.

Table 3
DAC performance at the critical input codes (Post-layout simulation)

Parameter	Mid-Code	Quarter-Code	RDAC-CDAC
V_{DIFF} at critical code (µV)	411.8	468.4	427.6
DNL (LSB)	-0.6063	-0.8272	-0.6682
Voltage settling time (ns)	400	400	400
Power consumption (mW)	0.1496	0.1303	0.1171

Generally, the deviations of the V_{DIFF} from the ideal voltage at the critical codes are mainly attributed to the conversion non-linearities brought about by the capacitor mismatches within the binary-weighted CDAC, which is well-founded by Liu *et al.,* [14] through their work. Despite the best efforts to induce an optimum device matching through the implementation of binary-weighted capacitors with minimum value of unit capacitance and area, the V_{DIFF} distortions and subsequent DNL errors are still inevitable due to limitations in the DAC routing and the aforementioned capacitor mismatch. This occurrence is further proven by Wen *et al.,* [16].

Meanwhile, the significant increase in the DNL levels during the post-layout simulation is indicative of the major degradation effect introduced by the layout parasites on the overall performance of the DAC. One of the main attributes of these parasites is the arrangement of the circuit components in a compact manner, which drain the vitals needed for optimal circuit performance. Furthermore, the adjacent conductive elements with varying charge levels creates an unnecessary capacitor within the DAC circuit. The resulting parasitic capacitance that is generated from this capacitor induces a charge differential between the plates and hinders the flow of electrons along the actual signal path. This in turn causes a decrement in the electron flux which adversely impacts the output signal integrity.

To reduce parasitic levels within the DAC, minimum-width metal wires should be implemented in the CDAC in accordance with the parasitic capacitance formula C= εA/D which states that the capacitance (C) is directly proportional to the area (A) of the metal plate or wire under observation. Conversely, the wirings within the RDAC are made thicker than their CDAC counterparts as wider wires pose lower levels of resistance to the flow of electric charge. In other words, wires with larger areas expedite a higher rate of charge and current flow within them which directly reduces the parasitic resistance levels of these wires.

In terms of power consumption, an optimal balanced must be reached between the trade-off relationship that exists between this variable and the voltage accuracy (represented by DNL errors). This would enable the DAC to attain minimum power consumptions while ensuring that the DNL errors are kept within acceptable levels. The simulation results in Table 3 show that the DAC acquires relatively low power outputs that dip below 0.15mW while maintaining DNL errors within the requisite +/- 1.0 range across all the critical input codes. Therefore, both the low-power and DNL error requirements of the DAC are fulfilled which indicates that the trade-offs between these

parameters have been leveraged at a balanced point. This result also justifies the selection of the DAC settings where a 2.1V VDDA specification and 10.0437pF unit capacitance were set for the entirety of the DAC simulation process.

3.4 Comparison with Previous Works

Table 4 depicts the comparison in performance between the proposed DAC and other circuitries of similar design and application purposes. The works selected for comparison possess essentially similar architectures, technologies, applications and key advancements as those of the proposed DAC.

The work carried out by Rikan *et al.,* [17] introduced a split-capacitor array that subdivided the 12-bit resolution into a segmented 8-MSB + 4-LSB CDAC, thereby reducing the number of capacitors and the power consumption within the circuit. Meanwhile, the segmented hybrid 5-bit thermometric capacitor array and 7-bit resistor string by Park *et al.,* [18] implemented a trimming algorithm to ensure that the DNL errors were reduced through a current compensation source. The employment of a residue boosting algorithm further managed to increase the resolution by a maximum of 2 bits without a noticeable increase in power consumption.

On the other hand, the self-calibrated trimming algorithm performed on the 14-bit DAC by Thirunakkarasu and Bakkaloglu [19] enabled the correction of majority of the circuitry mismatches, which helped to enhance the overall linearity of the design. Lastly, the sigma-delta DAC introduced by Ko *et al.,* [20] with a binary-weighted capacitor array achieves improved linearity and signal strength through the Dynamic Element Matching (DEM) technique. Furthermore, this method helps attenuate sampling noise while restoring the original DAC analogue output.

In this paper, the novel hybrid DAC is characterized by its high 14-bit resolution, which is the joint highest among all the works. Despite having slightly lower conversion frequencies than the works by Rikan *et al.,* [17] and Park *et al.,* [18], the proposed design compensates for this inferiority by attaining the lowest power consumption out of all the researched works. This is achieved via the implementation of a lower voltage supply for the operation of the DAC, thereby inducing a comparatively smaller power consumption than those of previous works. In terms of maximum performance improvements, the comparison made with the sigma-delta CDAC in the work by Ko *et al.,* [20] with similar process parameters has revealed a 563-time reduction in the power consumption by proposed DAC.

Furthermore, the implementation of the segmented architecture and the balancing of the trade-offs between power and linearity has facilitated stronger linearity performance in terms of DNL levels, which is lower or comparable to the works by Park *et al.,* [18] and Thirunakkarasu and Bakkaloglu [19] that incorporate similar input voltages, power consumptions and resolution levels. Generally, the overall designed circuit attains the desired 14-bit digital-to-analogue conversions while exhibiting low DNL and power consumptions under a relatively small supply voltage, thereby achieving the stipulated objectives of this work.

Table 4
Performance summary and comparison with previous works

Specification	Rikan *et al.,* [17]	Park *et al.,* [18]	Park *et al.,* [18]	Park *et al.,* [18]	Thirunakkarasu and Bakkaloglu [19]	Ko *et al.,* [20]	This work
Year	2021	2017	2017	2017	2015	2008	2020
Architecture	Split Type CDAC	Segmented Hybrid R-C	Segmented Hybrid R-C + Residue Boosting	Segmented Hybrid R-C + Residue Boosting	Self-Calibrated CDAC	Sigma-Delta CDAC	Segmented Hybrid R-C
Technology (µm)	0.13	0.065	0.065	0.065	0.6	0.18	0.18
Resolution (bit)	12	12	13	14	14	14	14
Supply (V)	2.7-5.5	1.6-3.6	1.6-3.6	1.6-3.6	15.0	3.0	2.1
Max. Frequency (MS/s)	5.0	4.0	3.5	2.0	0.4	-	2.5
Power (mW)	2.800	0.850	≈ 0.850	≈ 0.850	24.000	60	0.1496
DNL (LSB)	-	-0.55/0.39	-0.81/0.78	-0.88/0.95	0.92	-	-0.827

4. Conclusions

The paper presents a 14-bit differential hybrid Resistor-Capacitor DAC constituted of a 4-bit CDAC and 10-bit RDAC that is further subdivided into two separate 5-bit segmented strings. The implementation of this segmented array along with the binary-weighted capacitor design facilitates stronger conversion linearity within the DAC with the importance of a low-DNL output. The simulation results also indicate that the DAC achieves minimum power consumption due to the switching methods applied across both the sub-DACs. As the DAC is usually the largest occupant of area in high-resolution SAR ADCs, the matching precision of the DAC is a critical factor that impacts the overall linearity of the SAR ADC. Therefore, the acquisition of a well-matched circuit fits well in future SAR ADC research projects which integrates this component along with the SAR logic, comparator, and latch to attain high-resolution designs.

Nevertheless, the DAC research has been limited by the deterioration in linearity performance during the post-layout simulation which is indicated by a significant increase in the DNL levels. To overcome these challenges, future works could implement optimization methods such as input common mode voltage (VCM) based switching technique conducted by Zhu *et al.,* [21] that correlated the capacitors within the split-capacitor array during each bit transition to cancel out the error terms in the DNL, thereby contributing to a more accurate output voltage.

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References

[1] Xin, Xin, Jue Ping Cai, Teng Teng Chen, and Qi Di Yang. "A 0.4-V 10-bit 10-KS/s SAR ADC in 0.18 µm CMOS for low energy wireless senor network chip." *Microelectronics Journal* 83 (2019): 104-116. https://doi.org/10.1016/j.mejo.2018.11.017

[2] Ng, Mei Yee. "0.18 um low voltage 12-bit successive-approximation-register analog-to-digital converter (SAR ADC)." In *2011 3rd Asia Symposium on Quality Electronic Design (ASQED)*, pp. 277-281. IEEE, 2011. https://doi.org/10.1109/ASQED.2011.6111760

[3] Wei, Hegong, Chi-Hang Chan, U-Fat Chio, Sai-Weng Sin, U. Seng-Pan, Rui Paulo Martins, and Franco Maloberti. "An 8-b 400-MS/s 2-b-per-cycle SAR ADC with resistive DAC." *IEEE Journal of Solid-State Circuits* 47, no. 11 (2012): 2763-2772. https://doi.org/10.1109/JSSC.2012.2214181

[4] Xingyuan, Tong, Yang Yintang, Zhu Zhangming, and Liu Lianxi. "Novel hybrid D/A structures for high-resolution SAR ADCs-analysis, modeling and realization." *Microelectronics Journal* 42, no. 7 (2011): 929-935. https://doi.org/10.1016/j.mejo.2011.04.016

[5] Chen, Kairang, Martin Nielsen-Lönn, and Atila Alvandpour. "Asynchronous clock generator for a 14-bit two-stage pipelined SAR ADC in 0.18 µm CMOS." In *2016 IEEE Nordic Circuits and Systems Conference (NORCAS)*, pp. 1-4. IEEE, 2016. https://doi.org/10.1109/NORCHIP.2016.7792910

[6] Gaddam, Ravi Shankar, Kye-Shin Lee, and Chun Ki Kwon. "A 10-bit dual-plate sampling DAC with capacitor reuse on-chip reference voltage generator." *Microelectronics Journal* 44, no. 6 (2013): 511-518. https://doi.org/10.1016/j.mejo.2013.03.004

[7] Fan, H. U. A. "Effective method to improve linearity of high-resolution SAR ADC." *Microelectronics Journal* 61 (2017): 35-42. https://doi.org/10.1016/j.mejo.2016.12.010

[8] Ma, Bill, Qinjin Huang, and Fengqi Yu. "A 12-bit 1.74-mW 20-MS/s DAC with resistor-string and current-steering hybrid architecture." In *2015 28th IEEE International System-on-Chip Conference (SOCC)*, pp. 1-6. IEEE, 2015. https://doi.org/10.1109/SOCC.2015.7406897

[9] Kim, Mi-rim, Young-Ouk Kim, Yong-Sik Kwak, and Gil-Cho Ahn. "A 12-bit 200-kS/s SAR ADC with hybrid RC DAC." In *2014 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, pp. 185-188. IEEE, 2014. https://doi.org/10.1109/APCCAS.2014.7032752

[10] Jung, Dong-Kyu, Yun-Hwan Jung, Taegeun Yoo, Dong-Hyun Yoon, Bo-Yun Jung, Tony Tae-Hyoung Kim, and Kwang-Hyun Baek. "A 12-bit multi-channel RR DAC using a shared resistor string scheme for area-efficient display source driver." *IEEE Transactions on Circuits and Systems I: Regular Papers* 65, no. 11 (2018): 3688-3697. https://doi.org/10.1109/TCSI.2018.2854849

[11] Savitha, M., and R. Venkat Siva Reddy. "Dual split-three segment capacitor array Design Based Successive approximation ADC for Io-T ecosystem." *Integration* 69 (2019): 279-288. https://doi.org/10.1016/j.vlsi.2019.05.004

[12] Zhang, Yulin, Edoardo Bonizzoni, and Franco Maloberti. "A 10-b 200-kS/s 250-nA self-clocked coarse-fine SAR ADC." *IEEE Transactions on Circuits and Systems II: Express Briefs* 63, no. 10 (2016): 924-928. https://doi.org/10.1109/TCSII.2016.2538139

[13] Saberi, Mehdi, Reza Lotfi, Khalil Mafinezhad, and Wouter A. Serdijn. "Analysis of power consumption and linearity in capacitive digital-to-analog converters used in successive approximation ADCs." *IEEE Transactions on Circuits and Systems I: Regular Papers* 58, no. 8 (2011): 1736-1748. https://doi.org/10.1109/TCSI.2011.2107214

[14] Liu, Jianwei, Yan Zhu, Chi-Hang Chan, Sai-Weng Sin, U. Seng-Pan, and Rui Paulo da Silva Martins. "Uniform quantization theory-based linearity calibration for split capacitive DAC in an SAR ADC." *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 24, no. 7 (2016): 2603-2607. https://doi.org/10.1109/TVLSI.2015.2509164

[15] Sun, Lei, Bing Li, Alex KY Wong, Wai Tung Ng, and Kong Pang Pun. "A charge recycling SAR ADC with a LSB-down switching scheme." *IEEE Transactions on Circuits and Systems I: Regular Papers* 62, no. 2 (2014): 356-365. https://doi.org/10.1109/TCSI.2014.2363517

[16] Wen, Jiun-Yu, Pei-Hung Chang, Jhin-Fang Huang, and Wen-Cheng Lai. "Chip design of a 12-bit 5MS/s fully differential SAR ADC with resistor-capacitor array DAC technique for wireless application." In *2015 IEEE International Conference on Signal Processing, Communications and Computing (ICSPCC)*, pp. 1-4. IEEE, 2015. https://doi.org/10.1109/ICSPCC.2015.7338762

[17] Rikan, Behnam S., Arash Hejazi, DaeYoung Choi, Reza E. Rad, YoungGun Pu, and Kang-Yoon Lee. "12-Bit 5 MS/s SAR ADC with Split Type DAC for BLE." In *2021 18th International SoC Design Conference (ISOCC)*, pp. 125-126. IEEE, 2021. https://doi.org/10.1109/ISOCC53507.2021.9613993

[18] Park, Joonsung, Krishnaswamy Nagaraj, Mikel Ash, and Ajay Kumar. "A 12-/14-bit, 4/2MSPS, 0.085 mm 2 SAR ADC in 65nm using novel residue boosting." In *2017 IEEE Custom Integrated Circuits Conference (CICC)*, pp. 1-4. IEEE, 2017. https://doi.org/10.1109/CICC.2017.7993698

[19] Thirunakkarasu, Shankar, and Bertan Bakkaloglu. "Built-in self-calibration and digital-trim technique for 14-bit SAR ADCs achieving±1 LSB INL." *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 23, no. 5 (2014): 916-925. https://doi.org/10.1109/TVLSI.2014.2321761

[20] Ko, DongHyun, JiHoon Jung, YoungGun Pu, SangKyung Sung, KangYoon Lee, and Chul Nam. "A Design of 14-bits ADC and DAC for CODEC Applications in 0.18 µm CMOS Process." In *4th IEEE International Symposium on Electronic Design, Test and Applications (delta 2008)*, pp. 3-6. IEEE, 2008. https://doi.org/10.1109/DELTA.2008.124

[21] Zhu, Yan, Chi-Hang Chan, U-Fat Chio, Sai-Weng Sin, U. Seng-Pan, Rui Paulo Martins, and Franco Maloberti. "Split-SAR ADCs: Improved linearity with power and speed optimization." *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 22, no. 2 (2013): 372-383. https://doi.org/10.1109/TVLSI.2013.2242501