

Improvement of Power Quality in Smart Grid Connected P.V. System Using Multi-Level Inverter

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ARTICLE INFO	ABSTRACT
Article history: Received 4 April 2023 Received in revised form 14 May 2023 Accepted 15 May 2023 Available online 12 June 2023	This research proposed a cascaded multi-level inverter (CMLI) technique using Harris Hawk's Optimisation (HHO) for grid-connected P.V. systems. The photovoltaic (P.V.) system is connected to CMLI-isolated DC connections based on the relevant D.C. to D.C. converters. The main goal of the suggested approach is to control power or boost solar system energy conversion while maintaining power quality. CMLI is integrated into fewer switches, diodes, and sources to produce the best control signal with the suggested controller. To provide the best control signal data set for the CMLI, the gain parameter under the source's current normal value is assessed using the HHO. The proposed control theory and keeping the power factor constant control the active power fed to the grid. The suggested approach of integrating solar electricity into the
<i>Keywords:</i> DC-DC converters; Harris Hawks Optimisation (HHO); Particle Swarm Optimisation (PSO); Multi-level Inverters	grid using DC-DC converters and an asymmetric multi-level inverter structure is supported by the reduction in THD and active power to the grid. The suggested model is developed using the MATLAB/SIMULINK programme, and the experimental setup is used to validate the results. On the grid side, lower THD was attained, which complies with IEEE standards.

1. Introduction

Digital, electronic, and nonlinear devices controlled by microprocessors are widely used in all facets of the industry today. Almost all of these gadgets are susceptible to interruptions in the electrical supply at any time and cannot function effectively. In light of these facts, P.Q. has been increasingly crucial. Over the past few years, there has been a fourfold increase in the usage of sensitive loads, such as diagnostic equipment in hospitals, schools, jails, and other facilities, raising questions about their power quality [1-2]. The delicate and important loads must avoid these problems with power quality and voltage disturbances. Various solutions have been proposed in this area, including Custom Power Devices (CPDs), the best and most effective option for compensating for and reducing voltage fluctuations. Due to the rising demand for power worldwide and increased knowledge of environmental issues brought on due to the extensive use of fossil fuels, infiltration

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into renewable energy sources (RES) has expanded tremendously [3-4]. Photovoltaic (P.V.) energy is one of RES used to address energy issues globally, particularly in regions with abundant sunlight. It is currently heavily used to connect to the grid. Since the assurance to distribute regional burdens and the transmission of any extra PV-generated electricity to the grid, its grid connection form is quite effective.

Utilizing grid-connected solar and wind energy systems has greatly grown due to the rapid growth of power electronics and system methods [5-7]. In order to achieve successful power conversion based on RES, components like rectifiers, boost converters, and inverters are crucial [8]. Since the use of different inverters and loads, which are nonlinear, the grid experiences a variety of disruptions [9]. The harmonic of the gird current typically produces considerable heat and causes insulation degradation due to increased losses [10]. These variations cause ripples in torque, which causes vibrations in motors.

Additionally, unused reactive power reduces power factor and causes losses [11-13]. An unbalanced current can also result in losses and a neutral current. As a result, the harmonic content and reactive current restrictions of the P.V. system are not exceeded. Multi-level inverters, suited for conversion of medium and high power systems, are introduced to minimise loss and reduce harmonics [14–116]. The THD will be reduced as the level count is increased. A low THD output voltage is preferred, but adding more levels necessitates more circuitry and complicates control. Cost, high weight, complexity, and a good output voltage with lower THD are all tradeoffs. This study introduced a decreased switch level inverter with a two D.C. source for use with renewable energy sources [17-19]. The capacitor must be balanced properly to obtain the desired output voltage level. Both symmetric and asymmetric conditions are compatible with the suggested topology. The use of 'asymmetric' denotes that the voltage magnitudes of the D.C. sources are different.

A two-level inverter with four switches is the most basic topology that may be utilised for this conversion. There should be four anti-parallel diodes because each switch requires an anti-parallel diode. The output of a two-level inverter is a square-wave inverter output with more harmonics and necessitates the use of large filters to achieve a sinusoidal output shape [20]. The cost of the system is further enhanced by the high-size filters and insulation level required by conventional inverters, which place significant stress on switches (raising losses) and increase insulation density to withstand voltage stress. Multi-level inverters are created to overcome the drawbacks of traditional two-level inverters [21]. An electrical power device, a multi-level inverter, outputs a sinusoidal voltage output from an input number of D.C. sources. An electrical power inverter is a circuit that converts a D.C. to an A.C. signal, and the simplest topology that may be used for this conversion is the two-level inverter, which comprises four switches that form H-bridge. Since each switch needs an anti-parallel diode, hence results in four of them. A huge number of filters must be used in order to create a sinusoidal output form because the output of a normal two-level inverter is an inverted square wave with infinite harmonics [22]. The high-size filters and insulation level demanded by conventional inverters put a lot of strain on switches (increasing losses) and increase insulation density to withstand the voltage stress, which drives up the cost of the system.



Fig. 1. Block Diagram

2. Background of Research Work

A recent review based on P.V. power quality enhancement with MLI system shows power quality is a significant contributing component. Most recently, MLI advancements have concentrated on improving power quality and minimising the number of switches. The difficulties in deploying the control design are those based on power quality issues. Voltage fluctuations and safety-related issues cause issues in the utility system and lower the dependability and quality of the power. To solve these problems, MLI is used. Different MLI topologies, such as Cascaded Multi-level Inverters (CMLI) and Diode-Clamped Multi-level inverters (DCMLI), are now in use. Several methods address the power quality problem of the P.V. system with MLI. A fuzzy logic controller requires several data. It is equally feasible for programmes of all sizes, regardless of past data. The main drawbacks of genetic algorithms and particle swarm optimisation are their extremely slow processing speeds and inability to identify the best solution. For the best control of a grid-connected P.V. system, a very small number of control strategies have been proposed in the literature, but these strategies are not particularly effective [23-27]. These issues motivated us to conduct this investigation.

2.1 Circuit Description Considering Proposed System

Traditional power system topologies are changing due to the significant increase in the usage of environmentally friendly power sources (solar-based), producing reliability issues. At the right moment, reactive power problems and islanding related to renewables caused by high voltage variations (voltage droop & swell) are distribution networks' most serious power quality issues. Networks providing continuous electricity are strongly influenced by current quality and voltage drop.

3. Proposed Control Method

A sophisticated control mechanism should be applied to Cascaded H Bridge seven-level inverters to enhance the quality of grid currents and account for reactive power. By injecting harmonic current with a negative polarity with grid currents, improving or rectifying the current sine wave deformed due to harmonics introduced by nonlinear loads is possible. In addition to improving the current wave, voltage waveform distortions are also reduced. Using a nine-level H Bridge inverter to inject the reactive current needed by the load into the PCC, the reactive power strain on the grid caused by inductive loads can be decreased. As a result, this will increase the source-side power factor and lower losses sustained by other loads. These are the goals to take into account while selecting a control approach.

3.1. Modeling of Solar P.V. System

Generally, the solar system is incorporated into the P.V. module, dc-to-dc converter and load [29]. In order to get a certain value of Voltage and current from the solar module, the P.V. cells are arranged in parallel or in series. The solar cell forms a pn junction which uses the sunlight, creates the photocurrent and works as a diode in dark or shadows. The circuit model of the single-diode solar cell is shown in Figure 3.



Fig. 2. Outline about Proposed System



Fig. 3. Single diode model of P.V.

A diode and a resistor are incorporated into the current source. The mathematic expression of the P.V. characteristics is below,

$$i = i_{PH} - i_{Satu} \left(e^{\frac{v + iR_s}{q_f v_{Ther}}} - 1 \right)$$
(1)

Here, i_{satu} refers to diode saturation current, v_{Ther} refers to thermal Voltage, q_f refers to quality factor, i_{PH} denoted as light generated current. The light generated current is directly proportionate with the intensity of the light described by,

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$$i_{PH} = i_{Ther} \frac{i_{PHo}}{i_{to}}$$
(2)

Here, i_{to} refers to the standard intensity of light, i_{Pho} refers to the light current generating data open circuit condition,

$$i_{O} = i_{PH} - i_{Satu} e^{\left(\frac{qV_{openc}}{q_{f}v_{Therr}}\right)} - \frac{V_{openc}}{R_{ST}}$$
(3)

The reverse saturation current based on Eq. (3) is described by,

$$i_{Satu} = \left(i_{PH} - \frac{V_{Openc}}{R_{ST}}\right) e^{-\frac{-qV_{Openc}}{q_f v_{Ther}}}$$
(4)

The saturation current is derived by,

$$i_{o} = \left(\frac{i_{sc}(R_{se} + R_{sh}) - V_{oc}}{R_{sh}}\right) e^{\frac{-qV_{oc}}{nv_{t}}}$$
(5)

The MPP condition is applied and *I_{mpp}* is described by,

$$i_{mpp} = i_{PH} - \left(e^{\frac{q(V_{mpp} + i_{mpp}R_{SE})}{q_f v_{Ther}}} - 1\right) - \left(\frac{V_{mpp} + i_{mpp}R_{SE}}{R_{ST}}\right)$$
(6)

3.2 Boost Converter Model

To obtain the maximum power of P.V. boost converter is utilized. The maximal power point (MPP) is calculated depending on the converter's switching transistor duty cycle.

Figure 4 displays the circuit diagram of the boost converter [30-31]. The major contribution of the boost converter is that it converts the solar energy and boosts the solar energy. The maximized power obtained from the boost converter is given to the CMLI.



Fig. 4. Circuit diagram of the boost converter

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$$v_{o/p} = \frac{1}{1 - D_S} v_{i/p}$$
(7)

If $v_{o/p} > v_{i/p}$, then,

$$D_{S} = \frac{T_{on}}{T_{swit}}$$
(8)

Here, $v_{o/p}$, $v_{i/p}$ are the D.C. input and output voltage, on time period of semiconductor switch is denoted as T_{on} , switching period of semiconductor switch is denoted as T_{swit} . The boost inductor value is determined by,

$$l_{bo} = \frac{v_{i/p} D_S T_{swit}}{\Delta i_l} \tag{9}$$

Here, Δi_l is expressed as the inductor ripple.

Figure 5 indicates a multi-level inverter with fewer switches and a power switch IGBT is used. Table 1 indicates the switching states of power switches to get the desired output voltage of nine levels per the switching operation sequence [27].



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Switch	Operation	Table

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Switching Operation	Flow of Current	Combination	Output Voltage
		Voltage	
S ₃ ,S ₁ ,A ₁ ,B ₂ &B ₃	S ₃ -V ₁ -S ₁ -A ₁ -B ₂ -B ₃	V ₁	1v
S4,S1,V1,A2,B2&B3	S ₄ -V ₂ -S ₁ -V1-A ₂ -B ₂ -B ₃	V2-V1	2v
S ₄ ,V ₂ ,S ₂ ,A ₂ ,B ₂ &B ₃	S ₄ -V ₂ -S ₂ -A ₂ -B ₂ -B ₃	V ₂	3v
S4,V2,S2,V1,A1,B2&B3	S ₄ -V ₂ -S ₂ -V ₁ -A ₁ -B ₂ -B ₃	V2+V1	4v
S ₃ ,A ₂ ,B ₂ ,V ₀ &B ₃	S ₃ -A ₂ -B ₂ -V ₀ -B ₃	0	0
S ₃ ,A ₂ ,B ₁ ,V ₀ &B ₄	S ₃ -A ₂ -B ₁ -V ₀ -B ₄	0	0
S ₃ ,V ₁ ,A ₁ ,B ₁ &B ₄	S ₃ -V ₁ -A ₁ -B ₁ -B ₄	V1	-1v
S ₄ ,V ₂ ,S ₁ ,V ₁ ,A ₂ ,B ₁ &B ₄	S ₄ -V ₂ -S ₁ -V ₁ -A ₂ -B ₁ -B ₄	V2-V1	-2v
S4,V2,S2,A2,B1&B4	S4-V2-S2-A2-B1-B4	V2	-3v
S4,V2,S2,V1,A2,B1&B4	S4-V2-S2-V1-A2-B1-B4	V2+V1	-4v

4. Haris Hawk's Optimisation (HHO)

The Harris Hawk's algorithm, created in 2019, replicates the hunting behaviour of this sophisticated bird species that live in the USA [3,4]. These crafty birds use surprise in their hunting tactics. The leader and best-suited hawk in the group surrounds the prey after a group of hawks frighten it by simultaneously approaching their target (rabbits) from various angles. Three steps may be statistically distinguished between the way hawks grab their prey: (i) the Exploration Stage; (ii) the Stage that signals the transformation from exploration to exploitation; and (iii) the exploitation stage. The first phase is critical because it establishes the hawks' behaviour early in the attack. To begin with, each hawk selects a chance site at a high place to survey their surroundings and wait for its prey. When the prey looks closer, the corresponding hawks may attack it in several different methods, but only the leader will decide which tactic to employ. Depending on how the prey behaves, the hawks will either support and occupy the prey, or the leader will select one of them to receive the opportunity. Depending on the nearby hawk's location, the hawks may assume their positions for the two potential strategies.

$$X(t + 1) = (Xbest(t) - Xavg(t)) - \psi(LB + \tau(UB - LB)) \alpha < 0.5$$
(10)

$$X(t+1) = Xrand(t) - \beta |Xrand(t) - 2\varphi X(t)| \quad \alpha \ge 0.5$$
(11)

where Xbest(t) is the position of the chase (rabbits), X(t) is the position of the hawks at iteration t, X(t+1) is a vector representing the hawk's new positions in the upcoming iteration, and are distributed random numbers in the range of 0 to 1. The location variables' upper and lower bounds are indicated by the letters U.B. and L.B. A hawk chosen randomly from the current population is indicated by the notation Xrand(t), while the mean position of the hawks is shown by Xavg(t). The following formula is used to calculate the Hawks' typical position:

$$X_{avg}(t) = \frac{1}{N} \sum_{i=1}^{N} X_i(t)$$
(12)

N is the total number of hawks, and Xi (t) is each hawk's location in iteration t. HHO can change from exploring to exploiting depending on the prey's energy throughout the fleeing process. The following equation shows how the energy of the prey (rabbit) is calculated:

$$\mathbf{E} = 2\mathbf{x}\mathbf{E}_{\mathbf{0}}(1 - \frac{\mathbf{t}}{\mathbf{T}}) \tag{13}$$

where, the initial energy in each iteration is E0, which is randomly taken from [-1, 1], and T presents the maximum iterations.

The likelihood of an assault relies on whether the hawk has successfully discovered a prey as described in the earlier stages. If the prey manages to escape successfully, the probability of escape, or r, will be less than 0.5; otherwise, it will be greater than 0.5. Hawks either conduct a mild or severe siege, depending on their victim's route to flee. A severe or gentle siege will happen regardless of the energy of escape. When |E| is 0.5 and r is 0.5, the prey possesses sufficient energy to perform haphazard hops and cannot flee. In these pitiful attempts, the hawks circle the victim until it is worn out by their force, at which point they abruptly attack. The soft siege is thus defined as:

$$X(t+1) = \Delta X(t) - E | (J \times Xbest(t)) - X(t) |$$
(14)

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The difference between the prey's and hawks' positions in the present iteration is $\Delta X(t)$. The prey's random escape strength is J.

A hard siege will be performed when |E| < 0.5 and $r \ge 0.5$, as the prey has no energy to escape. Accordingly, the hawks hardly circle the prey to execute a surprise attack.



Fig. 6. Phases of HHO

HHO Steps:

- The population size and maximum number of iterations.
- Generate the initial population randomly.
- Check for stopping criteria.
- If the stopping criteria are not satisfied, then calculate the fitness value.
- For each hawk, set the prey location, update the value of E
- If |E|≥1, then it is the exploration
- If |E|<1, then it is exploitation
- Update location
- If $|E| \ge 0.5$ and $r \ge 0.5$ and then it is soft besiege
- Update location
- If |E|<0.5 and r ≥0.5 then it is hard besiege
- Update location
- If $|E| \ge 0.5$ 5and r < 0. then it is soft besiege with progressive rapid dives
- Update location
- If |E| < 0.5 and r < 0.5, then it is hard to besiege with progressive rapid dives
- position of prey and corresponding fitness is returned

5. Simulation Result

Nine level reduced switch topology inverter connected to grid for harmonics reduction is simulated and tested. Inverter input side is connected to its dedicated PV array consisting of one parallel string and seven series connected modules per string and other PV array consisting of one parallel string and twenty one series connected modules per string through boost converter. In detailed parameters of PV panel are given in table 2 Simulated system in MATLAB environment is shown in figure 7.



Fig. 7. Simulation Circuit

Table 2Simulation Parameters

P.V.	
The Open Circuit Voltage (Voc) is :	35.5 V
The Short Circuit Current (Isc) is :	8.52 A
The Voltage at maximum power point Vmp is:	28.63 V
The Current at maximum power point Imp is:	7.93 V
Series connected modules per string Ns1:	7
Parallel strings Np1:	1
Series connected modules per string Ns2:	21
Parallel strings Np2:	1
Grid	
Grid Voltage :	415V
Frequency:	50 Hz
Resistance Rg:	0.1 Ω
Inductance Lg:	0.05 mH

Load: In a nonlinear load and sag swell condition, taking HHO among the pi controllers into consideration is Non-sinusoidal current from the supply flows through resistance between the load and the power source in a nonlinear (non-sinusoidal) situation. Voltage dips are produced at each harmonic frequency as the appropriate harmonic current flows through the system impedance. Total voltage distortion is the sum of individual voltage drops, and the size of this distortion depends on the system impedance, the levels of system fault currents, and the levels of harmonic currents at each frequency harmonic.



Fig. 8. D.C. Voltages



Fig. 9. STATCOM Voltages





6. Experimental Results

The proposed method is done in simulation, and also an experimental prototype is implemented to confirm the simulation results are shown in Figure 11, control signals are in Figure 12 and Figure 13 and output voltage are in Figure 14 and Figure 15. Sinusoidal pulse width modulation generates control signals for switching power switches. The inverter's output voltage is successfully produced and filtered to get a sine wave, which results in lesser total harmonic distortion and meets with simulation results.



Fig. 11. Experimental Setup







Fig. 14. Output Voltage



Fig. 15. Output Voltage Sinusoidal

7. Conclusion

An efficient HHO technique is used in this study to enhance the quality of the power coming from the grid-connected P.V. system. The cascaded multi-level inverter utilised in the suggested system reduces the harmonics of the system. CMLI is incorporated into fewer switches, diodes, and sources with the suggested controller to generate the optimal control signal. The suggested method is implemented using the MATLAB/Simulink platform, and the method's effectiveness is compared to other approaches such as PSO-PI and P.I. The control signal for the CMLI is formed using the HHO approach. To analyse the suggested method, nonlinear load irradiation with temperature change is applied. An experimental prototype is put into use, and the results meet those of the simulation. The simulation produced THDs for the P.I. of 6.05%, 3.08%, and 1.65%.

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