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Hardware Implementation of FIR Filter for ECG Signal Processing: Design, Optimization, and Performance Analysis on an FPGA

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ABSTRACT

Electrocardiogram (ECG) signals are commonly used to diagnose heart-related diseases. However, noise induced during the measurement process can affect the accuracy of the diagnosis. Digital filters, such as the Finite Impulse Response (FIR) filter, are widely used to filter out noise from the ECG signal. Nevertheless, the processing speed of software-based FIR filters is slow for large ECG datasets due to serial processing. This paper presents a hardware implementation of the FIR filter for ECG signal processing to overcome the processing speed issue. The filter is designed using the Kaiser Window method and implemented on the Intel Cyclone IV Field Programmable Gate Array (FPGA). The filter is first designed in MATLAB to obtain the filter coefficients where the ECG data were obtained from Physionet database. From the difference equation, we designed the signal flow graph (SDFG) and then mapped into hardware logics to enable parallel processing. Simulation results of the software (MATLAB) and hardware (FPGA) implementations are obtained and compared. The results show that the FPGA-based FIR filter can process the ECG signal up to 1,250 times faster than software implementations. To further optimize the design and reduce hardware cost, we introduce optimized designs by applying the operation scheduling and constrained resource allocation techniques. The maximum operating frequency, logic utilization, and power consumption of each design were analysed and compared. This study demonstrates that custom-designed hardware logic for digital signal processing can significantly outperform software implementations due to its parallel processing capabilities. The proposed optimization techniques reduce the hardware cost while maintaining high processing speed and accuracy. The hardware implementation of the FIR filter for ECG signal processing has numerous applications in diagnosing heart-related diseases and real-time monitoring of ECG signals in critical care settings.

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1. Introduction

A pre-processing of a digital signal is a very important step in biomedical signal processing, especially to remove artifacts from the original signals [1]. ECG is one of the biomedical signals that is used to diagnose heart related diseases [2,3]. The ECG signal is measured using the sensors (electrodes) that are attached to the chest and limbs. During the measurements, the sensor not only detects the heart electrical signals, but also will pick-up noises as the sensors are also sensitive to electric and magnetic fields (EMF), especially the power line noise [4]. To remove those artifacts, the FIR filter is typically used as it has linear phase characteristics and has less distortions as compared to the conventional analogue filter [5,6].

Several filter designs for the ECG signal processing have been proposed. For example, Bhogeshwar *et al.*, proposed the Simulink model to denoise ECG signal using various IIR and FIR filters [4]. Their analysis shows that the FIR filter is the best filter for discarding the contaminated noises from the noisy ECG signals. Recently, more new techniques to improve the filtering performance were introduced. Mishra *et al.*, proposed an adaptive modelling [7] and denoising of ECG signal utilizing the second order FIR Notch filter to remove power line interference [8]. Usually, the FIR filter is used in other works as well, for example, Sumathi *et al.*, used the high pass least-square linear phase FIR filter to remove the artifacts from the original ECG signals in arrhythmia detection [9]. Other works that proposed the design of FIR filters for ECG signal filtering can be found in previous studies [10-13]. Most of the designs were implemented in the software environment such as MATLAB as it is a very comprehensive and convenient tool for digital signal processing. Experienced users can quickly design their own digital signal processing system. Though, inexperienced users can also utilize the signal processing toolbox with ease.

While software implementation provides a convenient tool for filter design, the serial processing nature of software might slow down the processing speed [14]. In other words, FIR filter algorithm implementation using a general-purpose processor running on a personal computer (PC) will not give the best performance in terms of processing speed. To speed up the processing speed, hardware implementations of the FIR filter have been proposed in many previous works[14-20]. Most of the designs were implemented on the FPGA as it offers flexibility in terms of reconfigurable. FIR filters can be implemented in a pipeline architecture, which can be easily parallelized to achieve high-speed processing. FPGAs are known for their high parallel processing capabilities, making them an ideal platform for implementing FIR filters [20-22]. It offers low-latency processing, which is crucial for real-time ECG signal processing applications. The low-latency processing of FPGA-based FIR filters enables the processing of ECG signals in real-time with high accuracy. Furthermore, as compared to software-based FIR filters, FPGA-based implementations consume less power [23,24]. This is because FPGAs have a specialized hardware architecture designed to perform specific tasks efficiently, whereas software-based implementations use general-purpose processors that are not optimized for specific tasks [25,26].

Although there were many works that have proposed hardware-based ECG FIR filter especially by using FPGA, most of the hardware designs were either synthesized using high-level synthesis tools or direct hardware mapping which are not optimized in term of speed, cost, and power consumption. In this work, we present several optimized hardware logic designs of an FIR filter for the ECG signal processing. The proposed design method can be applied to other FIR filter designs depending on the design requirements. The contribution of this work is the custom and optimized hardware design architecture of the FIR circuit for the application in ECG signal processing. The proposed circuit is mapped to the hardware based on the obtained difference equation and further optimized by applying operation scheduling which is implemented through our novel controller design. The circuit

is modelled using Verilog HDL with the Intel Cyclone IV FPGA as a targeted hardware. The design descriptions, experimental works, and results are presented in the subsequent sections.

2. Proposed Design

2.1 Software Implementation

The ECG data was obtained from the Physionet database which is one of the largest databases for complex physiologic signals. Figure 1 shows sample of ECG signals from the Physionet. The obtained ECG data is a raw ECG data, where it contains the original ECG signals and noises. The noise power components can be extracted by transforming the time domain ECG signals into a frequency domain representation using the Fast Fourier Transform (FFT) in MATLAB.

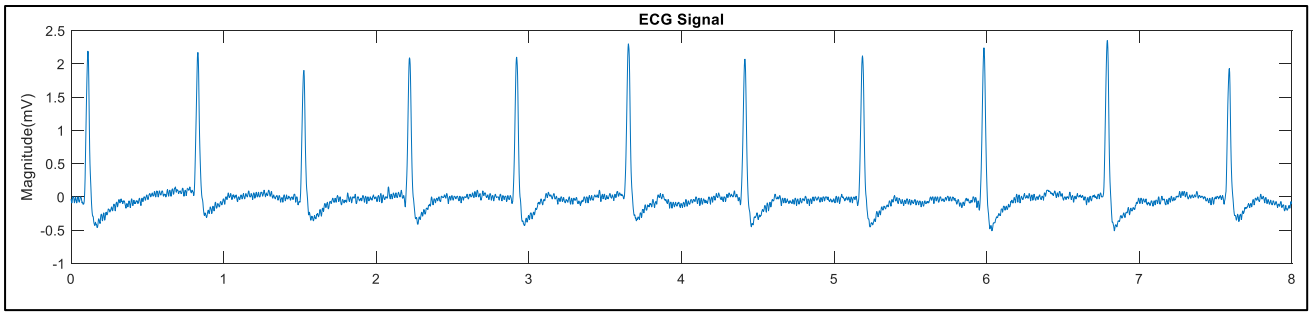


Fig. 1. ECG signal from Physionet

Figure 2 shows the frequency domain of the ECG signal that clearly shows the noise components. As the noises are mainly at the higher frequency (especially the power line noise at 60 Hz) as compared to the original ECG signal, therefore, the FIR lowpass filter can be designed to filter the noise out from the ECG signal. In this works, the FIR filter is designed using the Kaiser Window method defines by Eq. (1).

$$W_N[n] = \frac{I_0\left(\pi\beta\sqrt{1-4\left(\frac{n}{N-1}\right)^2}\right)}{I_0(\pi\beta)} \tag{1}$$

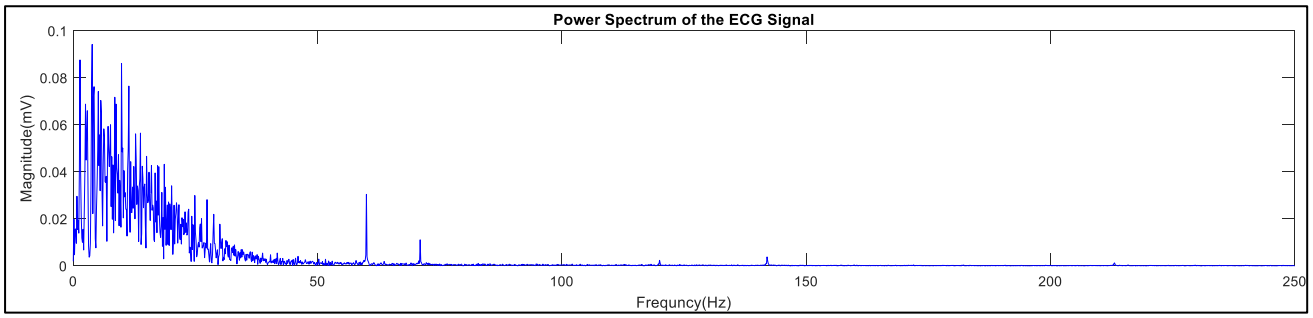


Fig. 2. Power spectrum of ECG signal showing noise components

where N is window length and $I_0(x)$ is the modified Bessel function of the first kind of order zero, given by Eq. (2).

$$I_0(x) = \sum_{k=0}^{x} \left[\frac{x/2^k}{k!}\right]^2 \quad (2)$$

The Kaiser window provides the designer considerable flexibility in meeting the filter specifications. In this work, the filter specifications were determined as follows: Sampling frequency = 500 Hz, cut-off frequency = 20 Hz, β = 3, filter length = 21 taps. The design produces the magnitude response as shown in Figure 3, where the output of the filtered ECG signal is given in Figure 4.

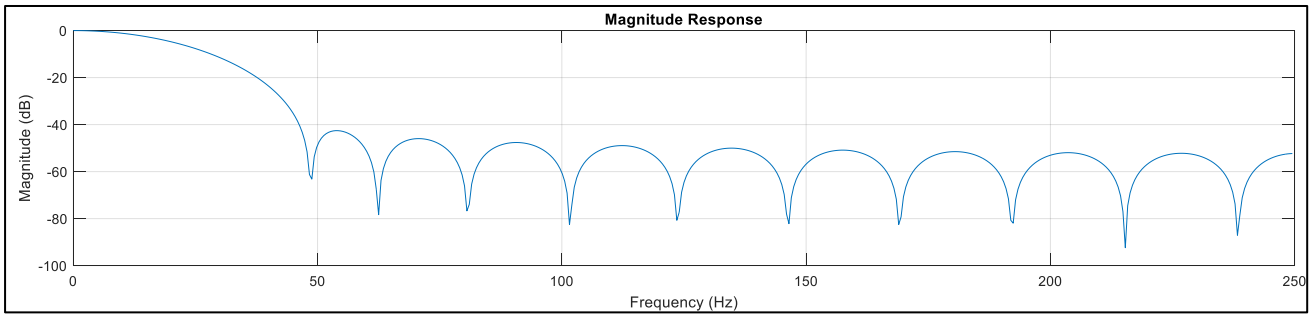


Fig. 3. Magnitude response of the designed filter

The difference equation of the proposed filter is given by Eq. (3). By substituting the coefficients that were obtained from MATLAB, Eq. (3) can be written as Eq. (4).

$$Y[n] = \sum_{i=0}^{K} b_i x(n-i) \quad (3)$$

$$Y[n] = 0.004375x(n) + 0.009402x(n-1) + \cdots + 0.004375x(n-20) \quad (4)$$

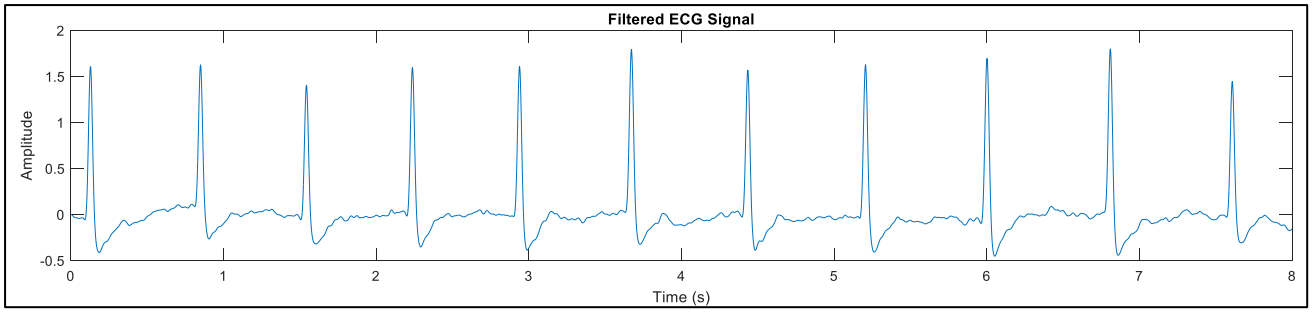


Fig. 4. Filtered ECG signal

The full coefficient values are given in Table 1. The coefficient values are also provided in fixed-point 16-bit digitized values, where these values will be used in the logic design.

Table 1
Filter coefficients

n	Coefficient value, b_n	Digitalized b_n
0	0.004375	287
1	0.009402	616
2	0.01675	1098
3	0.02634	1726
4	0.03775	2474
5	0.05023	3292
6	0.06276	4113
7	0.07417	4861
8	0.08332	5460
9	0.08925	5849
10	0.0913	5983
11	0.08925	5849
12	0.08332	5460
13	0.07417	4861
14	0.06276	4113
15	0.05023	3292
16	0.03775	2474
17	0.02634	1726
18	0.01675	1098
19	0.009402	616
20	0.004375	287

2.2 Hardware Implementation

2.2.1 Direct hardware mapping – Design 1

For the hardware implementation, Eq. (4) can be represented by the signal data flow graph (SDFG) as shown in Figure 5.

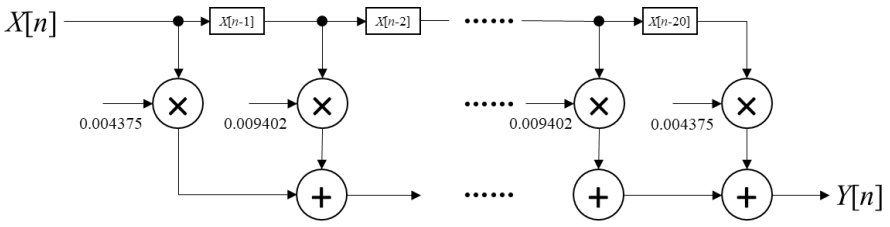


Fig. 5. SDFG of a proposed FIR filter

The SDFG is then mapped into the hardware logic design as illustrated in Figure 6. In our design, the memory is implemented to store the ECG data and the registers are used as the tab delay. The circuit is then modelled using the Verilog HDL in the Intel Quartus Prime where the targeted FPGA is the Intel Cyclone IV.

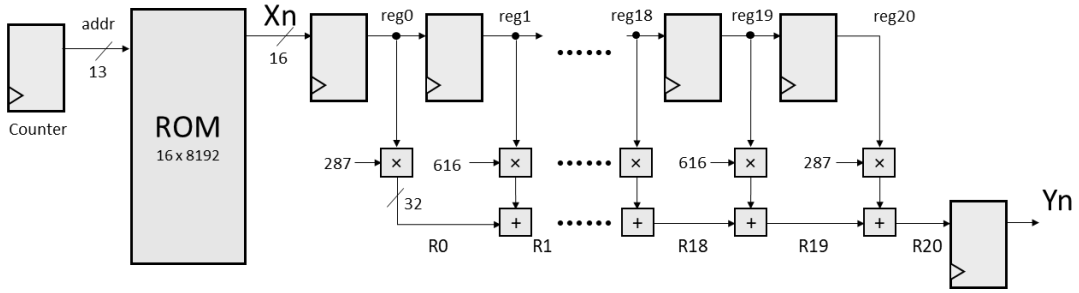


Fig. 6. Logic design of the proposed FIR filter

2.2.2 Results for direct hardware mapping design

We performed the simulation on the proposed FIR filter (Design 1) by using ModelSim. Meanwhile, the performance metrics were obtained from the design compilation report data provided by Intel Quartus Prime. Figure 7 shows the simulation result of the proposed hardware implementation of the FIR filter design. The signal on the top (*Xn*) is the input of the FIR filter (noisy ECG signal), while the bottom signal is the output (*Yn*). The result shows that the design works well where it produces the comparable output as displayed by software implementation in Figure 4.

Fig. 7. Simulation result of the proposed FIR filter design implemented on the Intel Cyclone IV FPGA

Table 2 provides the design performance metrics obtained from the Intel Quartus Prime compilation reports. As the design can run up to 50 MHz clock, this means the proposed hardware can produce the output at every 20 ns. Since there are 4000 data in the sample ECG signal, therefore, our design can filter the given ECG data in just 80 µs. This is almost 1,250 times faster than software implementation in MATLAB with measured elapse time of 0.1s running on a PC with AMD Ryzen 7 (3.2 GHz) processor and 16 GB RAM.

Table 2
Design performance metrics

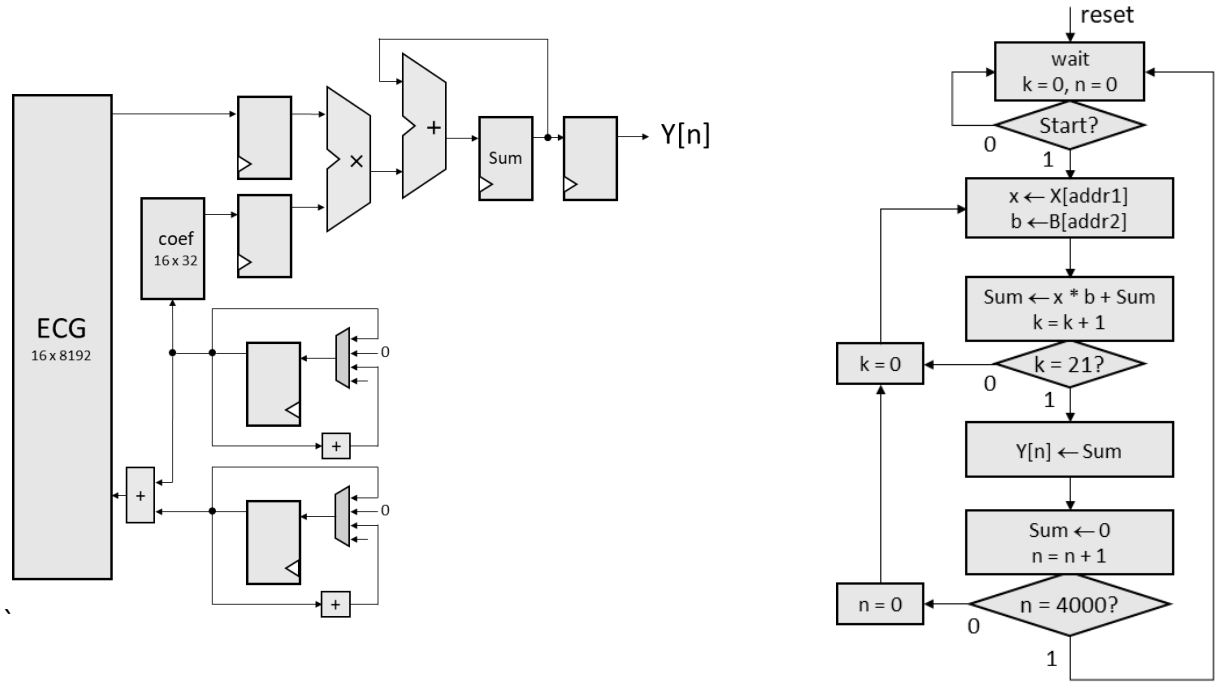
Design metrics	Reported data
Maximum operating frequency (Fmax)	50.66 MHz
Total logic elements	2,646
Total registers	381
Total memory bits	131,072
Total thermal power dissipation	93.47 mW

Although a substantially fast processing speed is achieved, we can observe that the logic utilization is quite high in this design, which is 2,646 logic elements out of 6,272 of the Cyclone IV logic resources. This is almost 42% of the total logic elements, resulting in high power consumption of 93.47 mW. The high logic utilization is due to the high number of multipliers (21 multipliers) in the design as the multiplier is an expensive circuit. To reduce the cost (logic elements), we now proposed a new design which the reduced number of multipliers as presented in the next section.

3. Optimized Hardware Design

3.1 Design 2

In this section, we present the optimized designs of the proposed ECG FIR filter hardware. To reduce the number of multipliers, we can implement operation scheduling and constrained resource allocation to the design. Figure 8 shows the design that is optimized for lowest cost where only one multiplier is utilized. Figure 8(a) shows the data path design of the FIR filter. In this design, the ECG data will be processed one at a time and will be accumulated in the accumulator, *Sum* before the output is produced at *Y*[*n*]. The operation and timing of the circuit are scheduled and controlled by a controller that is modelled by the arithmetic state machine (ASM) chart in Figure 8(b). This design will reduce the overall cost (logic elements) significantly as shown in the result section.



(a) (b)

Fig. 8. Design with one multiplier (a) FIR filter hardware design (b) Controller ASM chart

3.2 Design 3

Although the design presented in Figure 8 is the most cost-effective design, it also slows down the filtering process since it can only produce one output at a time. Nonetheless, with some modifications to the data path and controller, our operation scheduling method can enable concurrent computation of multiple computation units. Using this method, we were able to easily obtain a design with three multipliers, which will improve the speed of the ECG signal filtering process

while requiring a relatively low number of logic elements. Figure 9 and Figure 10 depict the data path design and the ASM chart of the controller for this design, respectively.

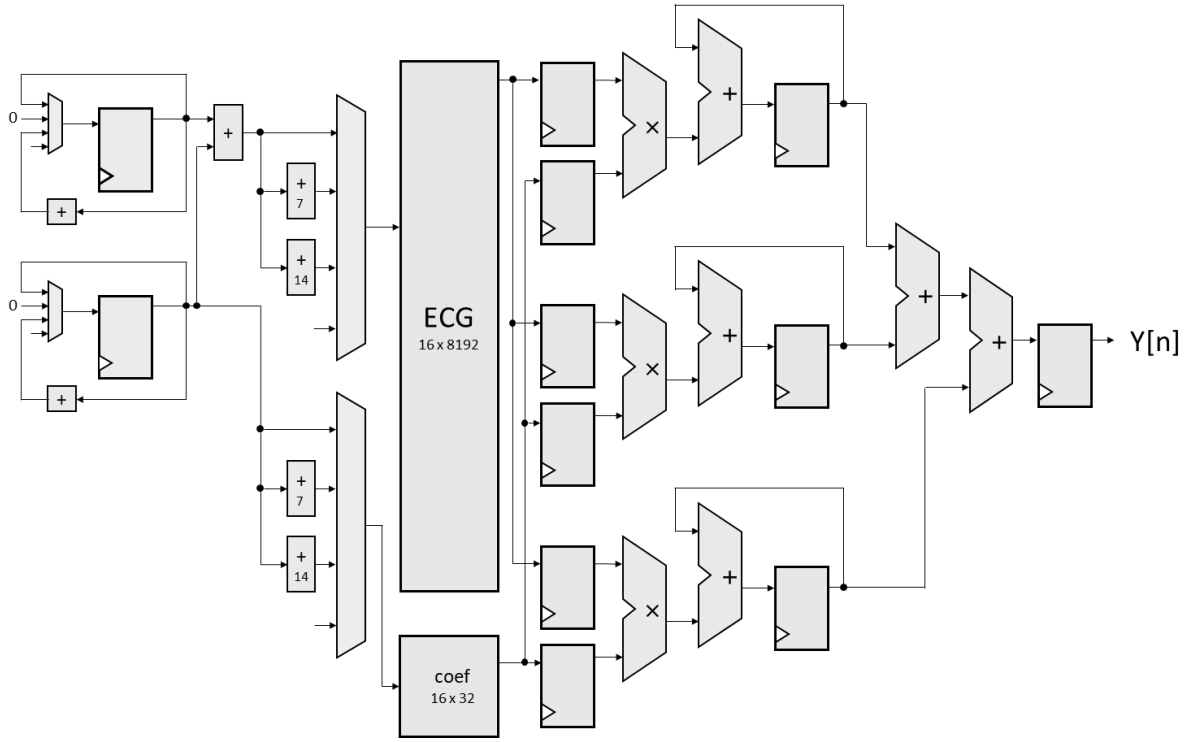


Fig. 9. Datapath design of a FIR filter with three multipliers

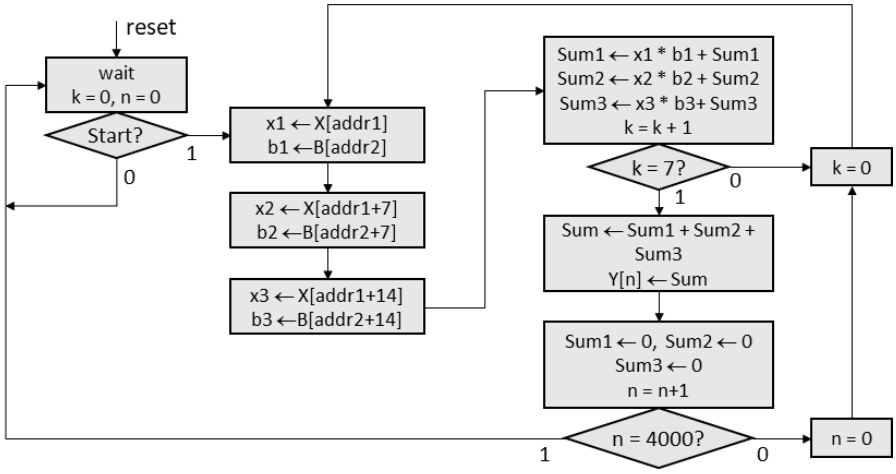


Fig. 10. Controller ASM chart for a FIR filter with three multipliers design

4. Results and Analysis

This section presents the results and analysis of the experiments conducted on all designs. Figure 11 and Figure 12 display the simulation results for the ECG FIR filter with one multiplier and three multipliers, respectively.

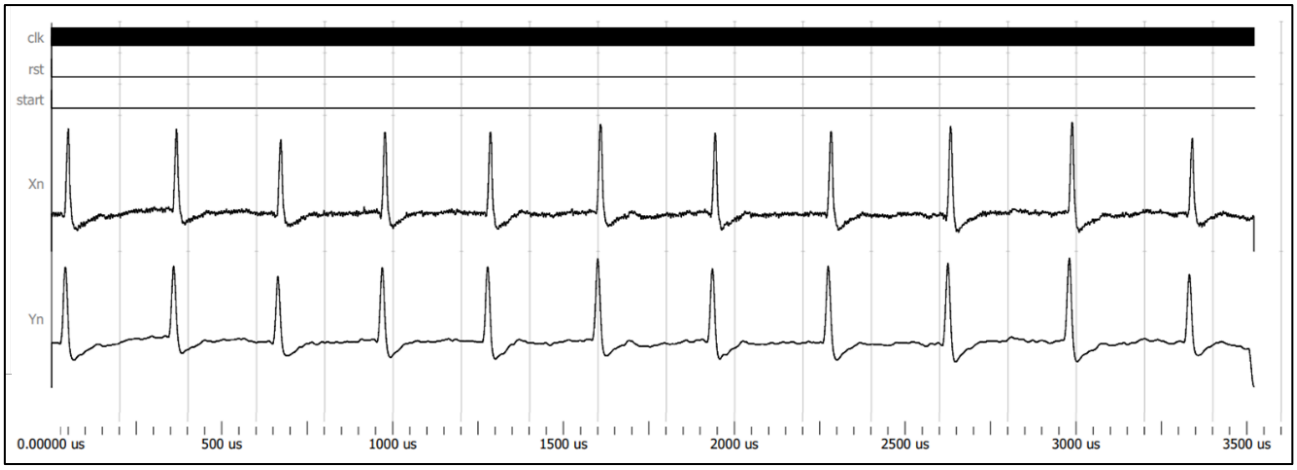


Fig. 11. Simulation result of the ECG FIR filter Design 2

Fig. 12. Simulation result of the ECG FIR filter Design 3

Table 3 summarizes the performance metrics of each design. The results indicate that all hardware designs outperform the software implementation in terms of processing speed. Even the one-multiplier design, which computes data sequentially, is 28 times faster than the software implementation. It is important to note that the hardware implementation on the FPGA runs at a much lower frequency (50 MHz) than the software implementation (3.2 GHz). The maximum operating frequency can be increased by using a faster FPGA device. In this work, all hardware designs were simulated at a 50 MHz clock. From the results, it can be seen that the one-multiplier design is the most cost-effective option, utilizing only 145 logic elements, which is only 2% of the total logic elements in the FPGA. This is a significant improvement compared to the fully parallel design (Design 1), which requires 2,646 logic elements (42%). Moreover, this design also demonstrates improved power consumption, reducing it from 93.47 mW to 74.06 mW. The three-multiplier ECG FIR filter design demonstrates a processing speed improvement of 28% over the one-multiplier design, while only requiring a slight increase in the number of logic elements from 145 to 290, which is considered low.

Table 3
Performance comparison

Performance metrics	Software	Design1	Design2	Design3
Speed	100,000 µs	80 µs	3,500 µs	2,500 µs
Maximum operating frequency	3.2 GHz	50.66 MHz	80.22 MHz	80.21 MHz
Total logic elements	-	2,646	145	290
Total registers	-	381	95	161
Total memory bits	-	131,072	131584	131,584
Total thermal power dissipation	-	93.47 mW	74.06 mW	73.49 mW

Furthermore, to prove that the proposed design work for different ECG data, we also performed the test on other ECG signals from Physionet. The test results are given in Figure 13.

Fig. 13. Test for other ECG data from Physionet

5. Conclusions

In this study, we presented the designs of FIR filters for ECG signal processing and implemented them on an FPGA to accelerate the filtering process for large volumes of ECG data. The main contribution of this work is the development of a novel and optimized hardware architecture for FIR filters in ECG signal processing. Our design technique can be customized to meet various design requirements and is applicable to other FIR filter designs for different applications. The results demonstrate that the proposed design significantly outperforms the software implementation in MATLAB running on a general-purpose processor in a PC. We have demonstrated that the proposed design can be optimized for cost-performance trade-off, as presented in designs 1 and 2. In future

work, we plan to explore other design configurations, such as logic transformation and constrained resource allocation, to further reduce the design cost and overall circuit power consumption.

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