SEMARAK ILMU PUBLISHING

Journal of Advanced Research in Applied Sciences and Engineering Technology

Journal homepage:
https://semarakilmu.com.my/journals/index.php/applied_sciences_eng_tech/index
ISSN: 2462-1943

All Solution Processable OTFT-Based on Direct-Written Printing Method Towards Flexible Electronics Applications

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ARTICLE INFO

Article history:
Received 22 June 2023
Received in revised form 28 October 2023
Accepted 1 November 2023
Available online 20 March 2024

Keywords:
Organic thin film transistor; Direct-write printing; TIPS-PEN; Semiconductor devices

ABSTRACT

Development of organic electronics, particularly organic thin film transistors (OTFTs), have been centred of discussion among researchers due to their potential uses in flexible electronics applications. Conventionally, an inkjet printing method has been deployed to fabricate the OTFTs due to its simplicity in fabrication steps and applicability to diverse substrates and solution-processable materials. Nonetheless, this technique has a major drawback which requires low viscosity materials to prevent clogging issue at the printer's nozzle. This in return limits the material selections and requires additional steps i.e., modification of the selected materials to fit the printer's requirement or in other words, to avoid clogging at the nozzle. Therefore, this paper proposes a method to fabricate a bottom gate bottom contact (BGBC) OTFT by using a direct-write printing technique which is compatible with a commercial conductive ink that can be directly used without any further modification. This technique does not compromise the fabricated devices overall performance and can fabricate the devices up to micrometre scale. The proposed OTFT achieved a saturation mobility of 4.28 x 10^{-5} cm^2/Vs, a threshold voltage of -0.4 V, an on/off current ratio of 10^2, and a subthreshold swing of 10 mV/dec with overall fabrication temperature is less than 150 °C, hence, makes it suitable for flexible electronics applications.

1. Introduction

The development of organic thin film transistors (OTFTs) has been thoroughly studied recently due to the growth of the printed electronics industry over the past decades. To ensure their competitiveness against the other stable silicon-based transistors, these next generation of electronic devices are required to be light-weighted, multi-functional, flexible, low-cost, and possess simple fabrication process as listed in [1].

A wide range of deposition and patterning techniques have been established by researchers, mostly are contact (e.g. photolithography and screen printing) and non-contact (e.g., inkjet printing

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https://doi.org/10.37934/araset.41.2.93101

and direct ink writing) methods as mentioned Yusof *et al.,* [2]. Among these methods, the latter is most likely to be adopted by researchers since it has high compatibility with various substrates, solution processable materials, and low processing temperature, making it suitable for flexible electronics applications. On top of that, this technique excludes etching and lift-off processes, which makes the fabrication process easier and cheaper.

Furthermore, an inkjet printing technology has been widely explored by researchers to develop flexible electronic devices. Despite on being the leading choice in realizing all-solution processable OTFTs, the effort to fully commercialize the OTFTs becomes stagnant due to its clogging issue and restriction in material selection since the inkjet printer can only work with low-viscosity ink as be pointed in [1], [3].

To resolve these issues, researchers started to adopt three-dimensional (3D) printing in fabricating flexible printed electronics. Initially, 3D printing is used for rapid prototyping molds and tooling, digital manufacturing, and individual fabrication. The rapid progress in technology has broadened its applications towards flexible electronics. A direct-write assembly or printing (DIW) based on 3D printing technology has been utilized to print the conductive grids for tissue engineering and cell culture applications as done in [4-6] which serves as a completely new bottom-up manufacturing technique to fabricate electronic devices. Besides, DIW printing method has been used to deposit electrodes for electronic devices such as diodes and light-emitting diodes (LEDs) as indicated by Hou *et al.,* [1] and is yet to be explored for OTFTs applications.

As one of the important layers in the OTFT structure, the organic semiconducting layer influences the performance of the OTFT in terms of the charge carrier mobility. Molecule-based semiconductors including conjugated polymers and small molecules have been used by researchers as the organic semiconducting layer since both are solution processable materials. Nevertheless, the conjugated polymers showed inferior performance due to their natural vulnerability towards oxygen in the inert condition as proven by Kehrer *et al.,* in [7]. On the other hand, the OTFTs based on small molecule conducting layer demonstrated better electrical and morphological performances. 6,13-bis(triisopropylsilylethynyl) pentacene (TIPS-PEN) is one of the small molecule materials that has been comprehensively used due to its relatively high carrier mobility and stability as shown in [8]–[11]. Although thermal evaporation has been exploited to deposit the organic semiconducting layer as done by Scuito *et al.,* in [11], this technique is however incompatible with flexible substrate and possessed complex procedures. Thus, a spin-coating technique is more preferrable due to its simplicity and can work well with solution processable materials as shown in [12].

In this work, we successfully reported a room-temperature, printed and all-solution-processable OTFT using silver nanoparticle (AgNP), silicon dioxide (SiO_2), and 6,13-bis(triisopropylsilylethynyl) pentacene (TIPS-PEN) as the source/drain electrodes, gate dielectric, and organic semiconducting (OSC) layers, respectively on silicon wafer. The conductive ink was used without further modification. This work able to manufacture an OTFT up to micrometer size channel length using the DIW printing technique without compromising its overall performance.

The rest of the paper is structured as follows: Section 2 describes in depth the materials and experimental details in fabricating and characterizing the BGBC OTFT. Next, Section 3 analyses the fabricated devices electrical and morphological characterization results. These results have been discussed intensively and compared with previous works if applicable. Lastly, Section 4 concludes the paper.

2. Materials and Experimental Details

2.1 Materials

The materials used in this work consist of an off-the-shelf silver nanoparticle (AgNP) conductive ink without any further purification for the Source and Drain (S/D) electrodes. A high purity > 99.9 % of 6,13-Bis(triisopropylsilylethynyl)pentacene (TIPS-PEN) was used as the Organic Semiconductor (OSC) layer, which purchased from Ossila Ltd without further purification. While the solvent for the TIPS-PEN i.e., Toluene with 99.5 % AR Grade was purchased from Chemiz (M) Sdn. Bhd. Finally, the substrate used in this work is a Si-wafer (p-doped) with a thermally grown SiO_2 dielectric layer.

2.2 Experimental Details

This section consists of two main parts – device fabrication using DIW printing technique, followed by the electrical and morphological characterizations of the fabricated devices. Note that, BGBC OTFT was fabricated using all solution-processable materials. Furthermore, the fabrication and measurement were carried under room temperature.

2.2.1 Fabrication of all solution processable OTFTs

Firstly, the substrate was cleaned by a standard solvent-cleaning process using acetone, isopropyl alcohol (IPA), and deionized (D/I) water sequentially in an ultrasonic bath for 3 min each. The substrate was dried using a dryer to evaporate the residual solvent and moisture. Subsequently, the substrate was loaded to the printer's tray. This work used Voltera's V-One DIW printer and all the conductive OTFT layouts were designed using CAD software. Figure 1 shows the layout of the conductive source/drain patterns of the OTFT. The designs were exported as Gerber files before they were uploaded to the Voltera's software interface to be printed. Before starting any printing process, the designed pattern was outlined on the substrate using the probe and its height was measured to avoid crashing between the nozzle and the substrate. The AgNP conductive ink was injected into the cartridge and primed before it was ready to be used. The printing parameters were adjusted successively, including the kick and the rheological setpoint before the designed pattern was ready to be printed. Finally, the printed patterns were cured on the printer's heated bed at temperature between 100 ℃ to 150 ℃ for 1 hour. Figure 2 depicts the DIW printing method of the OTFTs source/drain conductive patterns.

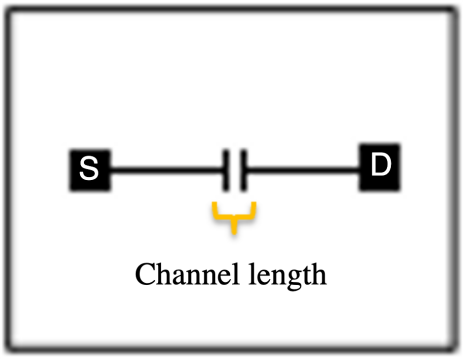


Fig. 1. Layout of the conductive source/drain contacts of the OTFT

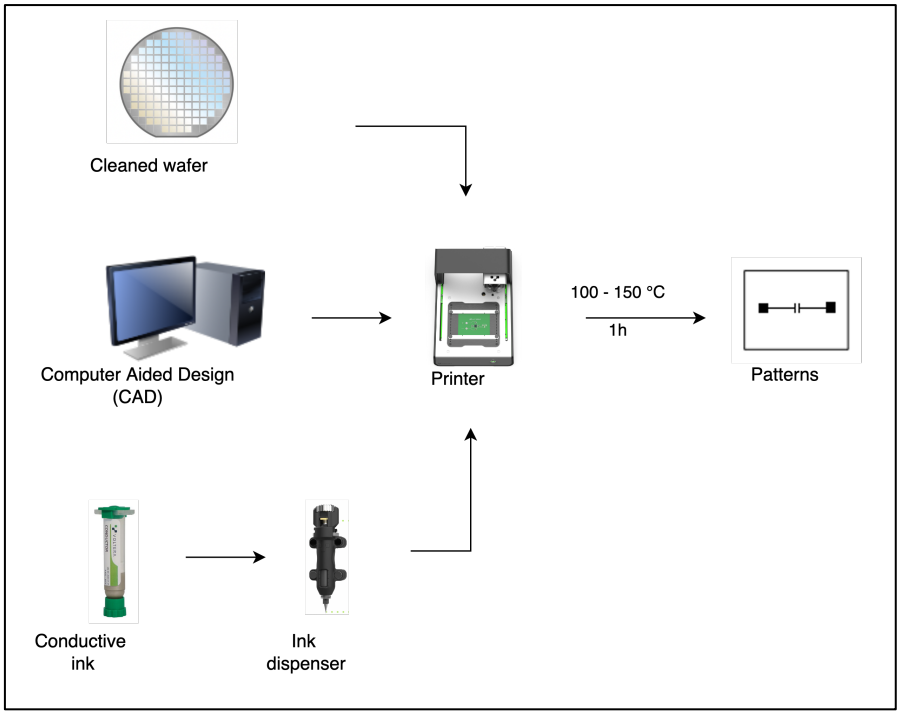


Fig. 2. DIW printing method of the conductive source/drain patterns

Next, to complete the OTFT structure, the OSC layer was deposited on the conductive patterns. The OSC solution was prepared by dissolving TIPS-PEN in Toluene. This solution was heated between 60 ℃ to 100 ℃ for 1 hour on a hot plate with magnetic stirrer to dissolve all the particles. The TIPS-PEN solution was then deposited on the conductive source/drain patterns by a spin-coating technique, whereby the spin-coater profile had been optimized to ensure a thin and uniform film formed on the substrate. Subsequently, the sample was annealed between 80 ℃ to 100 ℃ for 10 min to remove any access liquid. At the end of the fabrication process, the sample was then cleaned with a cotton swab wetted with Toluene to remove any excess semiconductor on the sample's surface except at the channel area.

2.2.2 Electrical and morphological characterization of the OTFTs

The OTFTs were characterized and analyzed using a Keithley 4200 semiconductor analyzer and a quick test system consisting of a custom probe station and optical microscope. The thickness of the deposited S/D layer was measured using a KLA-Tencor Alpha-Step® D-100 profilometer while the scanning electron microscopy (SEM) was used to measure the OSC layer thickness. As for the OTFTs images, they were captured by an Olympus BX61 motorized optical microscope.

3. Results and Discussion

Figure 3(a) illustrates the schematic cross-sectional view of the fabricated OTFT device on Si substrate, while Figure 3(b) and (c) show the camera photograph of the DIW-printed TIPS-PEN based OTFT device and the optical microscopy image of the fabricated OTFT, respectively. The conductive S/D contacts of ~1210 µm were DIW-printed, while the OSC layer of ~30 nm was spin-coated.

Although works have been done using DIW printing method to develop sensors and electronics circuits as can be seen in [1], nevertheless limited number of research can be found on utilizing this technique to deposit electrodes for organic transistor applications. Hence, this work had successfully

employed DIW printing method to deposit S/D contact as shown in Figure 3(b). On top of that, this technique can fabricate the OTFT with channel length up to micrometre size without additional parts (e.g., AFM-coupled dip-pen nanolithography and meniscus-guided pen) as work done by other researchers in [13]. The approximate channel length of the fabricated OTFT was 0.5 µm as shown in Figure 3(c).

As a versatile printing technology, DIW method is compatible with many types of inks, including nanoparticle conductive inks. This work chose the AgNP conductive ink because it has a relatively narrow hole Schottky barrier with TIPS-PEN. The reported work functions of AgNP electrodes and TIPS-PEN were 4.93 eV and 5.3 eV, respectively as in [8-9]. Therefore, the resulting energy gap of 0.37 eV is achieved between these two materials, as shown in Figure 4. The narrow barrier between the electrode and semiconductor is necessary to promote hole injection as mentioned by Wageh *et al.,* in [16]. In addition, AgNP is the best candidate for the electrode since it has a lower curing temperature (< 150 ℃) as compared to gold (> 190 ℃), making it suitable for flexible substrate electronics.

Apart from that, Toluene was chosen as the solvent for TIPS-PEN, because high boiling point of the Toluene allows the solvent to evaporate slowly after the deposition of the TIPS-PEN solution. This is important to ensure that a highly ordered molecule structure is formed after the solvent evaporates completely as notified by Kim *et al.,* in [17]. As a result, a uniform thin-film layer of OSC with ~30 nm thickness was formed on the dielectric layer as demonstrated in Figure 5. Moreover, the maximum device fabrication temperature was kept below 150 ℃, making it compatible with flexible electronics applications.

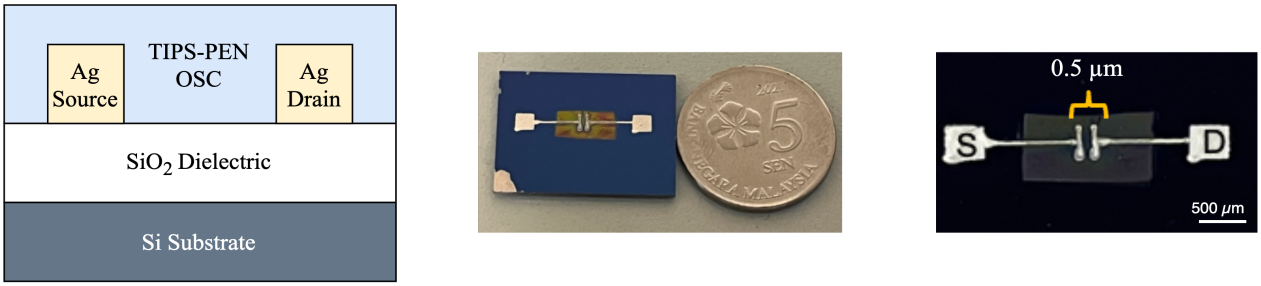


Fig. 3. (a) Schematic cross-sectional view of the fabricated OTFT device, (b) camera photograph of the DIW-printed TIPS-PEN based OTFT device fabricated on Si substrate, and (c) optical microscope image of a single OTFT device with the scale bar 500 µm in length

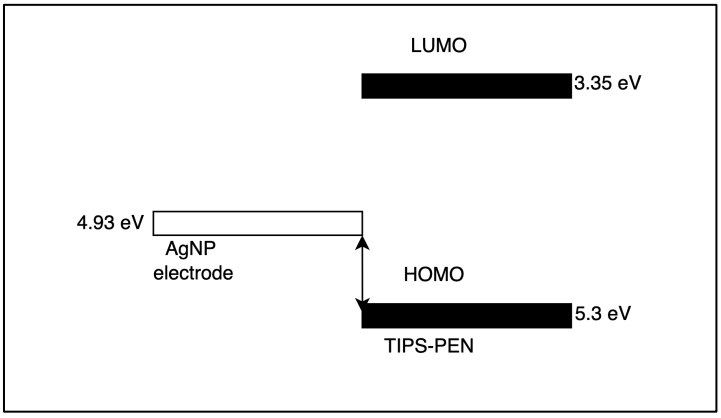
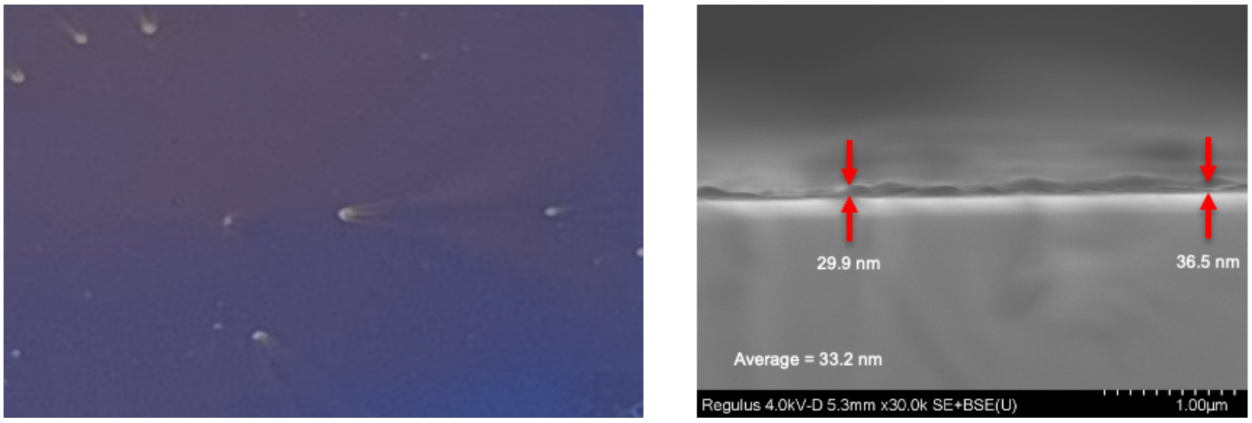


Fig. 4. Work function of AgNP electrode and the energy levels (LUMO and HOMO) of TIPS-PEN



(a) (b)

Fig. 5. (a) Optical microscope image and **(b)** SEM image for spin-coated TIPS-PEN active layer on SiO_2 dielectric layer

Figure 6(a) and (b) show the output characteristics (I_{DS}-V_{DS}) and the transfer characteristics ($|I_{DS}|$-V_{GS}) of the BGBC OTFT, exhibiting a typical p-type field effect transistor behaviour. V_{DS} was varied from 0 to -60 V with -5 V increment at different V_{GS} ranging from 0 to -20 V. Negative voltages have been applied since holes are the majority charge carriers in TIPS-PEN. The extracted saturation mobility μ_{sat} is about 4.28 x 10^{-5} cm^2/Vs, the threshold voltage V_{th} of -0.4 V and the on/off current ratio (I_{ON}/I_{OFF}) up to 10^2 (V_{GS} = -20 V and V_{DS} = -40 V) were achieved. The proposed OTFT performance is on par as achieved by Ramon *et al.,* in [18]. Nevertheless, the OTFT exhibits high OFF current of 10^{-8} A, possibly due to a high leakage current in the oxide. The field effect mobility of the OTFT at saturation region was calculated as in Eq. (1) as done in [19].

$$\mu_{sat} = \frac{L}{W}\frac{1}{C_i}\frac{\delta^2 I_{DS}}{\delta V_{GS}{}^2} \quad (1)$$

Where μ_{sat} is the saturation mobility, C_i is the geometric capacitance of the dielectric, while L and W are the channel length and width, respectively. High mobility is needed to ensure fast switching speed in the transistor which is highly dependent on the quality of deposited OSC layers. The sub-threshold swing SS of 10 mV/decade confirms the good interface formed between dielectric and OSC layers. This can be achieved by having a low deep gap states localized near the semiconductor/dielectric interface. The SS value was calculated from the inverse subthreshold slope using Eq. (2) as described in [16], [20]. The overall performance matrices of the proposed OTFT are summarized in Table 1.

$$SS = \frac{dV_{GS}}{d(logI_{DS})} \quad (2)$$

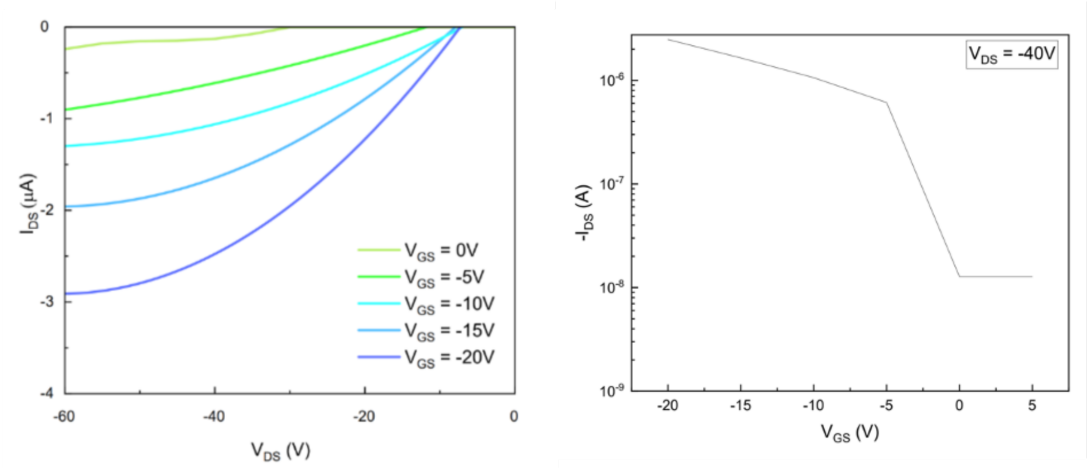


Fig. 6. Characteristics of BGBC OTFT: **(a)** Output (I_{DS}-V_{DS}) and **(b)** transfer ($|I_{DS}|$-V_{GS}) characteristics

The overall performance of the fabricated device is comparable with those fabricated using an inkjet printing method. Although the achieved μ_{sat} is lower than in other research , nevertheless it can be further improved by optimizing the deposition technique of the OSC layer. Besides, this work demonstrated the best V_{th} of less than -0.5 V as compared to the other works. In short, based on the results summarized in Table 1, it can be confirmed that DIW printing technique can be utilized to fabricate the OTFTs up to micrometre scale and can be further explore to improve the electrical performance of the OTFTs.

Table 1
Comparison of the OTFT performance with the other state-of-the-art works

Reference	[16]	[18]	[21]	**This work**
S/D Deposition Technique	Inkjet-printed	Inkjet-printed	Inkjet-printed	**DIW-printed**
OSC Layer	F8T2	FS0027	TIPS-PEN	**TIPS-PEN**
Saturation Mobility μ_{sat} (cm^2/Vs)	9.70 x 10^{-3}	1.90 x 10^{-4}	6.50 x 10^{-2}	**4.28 x 10^{-5}**
Threshold Voltage V_{th} (V)	-12.50	-0.90	1.24	**-0.40**
On/Off Current Ratio I_{ON}/I_{OFF}	10^2	10^2	10^3	**10^2**
Subthreshold Swing SS (mV/decade)	37.8	-	-	**10**

4. Conclusions

Deposition of electrodes using DIW-printed technique and fabrication of the OTFT using all solution processable materials can be reflected as a competitive technique presently. Although many works have utilized an inkjet-printed method to fabricate the OTFTs, its nozzle's clogging issue has slowed the progress of the OTFTs. Thus, in this work, we demonstrated all solution processable OTFTs with channel lengths up to micrometre scale by using DIW-printed method. Notably, the proposed OTFT exhibited a saturation mobility of 4.28 x 10^{-5} cm^2/Vs, a threshold voltage of -0.4 V, an on/off current ratio of 10^2, and a subthreshold swing up to 10 mV/decade. Besides, the overall processing temperature was kept below 150 °C to suit flexible substrate requirements. Thus, we believe that by

using narrow DIW-printed electrodes with low annealing condition, this method can be widely explore for low-cost and low voltage flexible electronics applications.

Acknowledgement

This research was funded by Ministry Of Higher Education Malaysia for Fundamental Research Grant Scheme with Project code: FRGS/1/2020/TK0/USM/02/30. The authors also would like to express gratitude to USM School of Electrical and Electronic Engineering Semiconductor Lab (SEEE Semiconductor Lab) for the research facilities to conduct the research.

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