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A 2.4/5.2 GHz Concurrent Dual Band Low Noise Amplifier with Forward Body Bias Technique for WLAN Applications

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Keywords:

Dual band; Low noise amplifier; Forward body bias; WLAN

ABSTRACT

This study describes a dual band LNA CMOS developed for a Wireless Local Area Network (WLAN) application using CMOS 0.13-m Silterra technology. One of the most difficult aspects of creating dual band LNA is striking a balance between gain and noise figure over both frequency bands. Consequently, the suggested design integrates forward body bias approach with cascode topology and source degenerate inductor to optimize the result achieved. The simulation results show a total power consumption of 5.8 mW at 0.6 V supply voltage, with a gain of 16.1 dB at 2.4 GHz and 14.9 dB at 5.2 GHz. Furthermore, at 2.4 GHz and 5.2 GHz, input return loss was -23.7 dB and -14.9 dB, with noise values of 2.7 dBm and 1.7 dBm, respectively. Overall, this study helps to create dual band LNA designs for WLAN applications.

1. Introduction

WLAN is a type of wireless communication that allows devices to connect to a local network and the internet without the need for physical cables [1]. It is commonly used in homes, offices, public spaces, and various other environments to provide wireless connectivity to devices like smartphones, laptops, tablets, and IoT (Internet of Things) devices. WLAN devices operate using different frequency bands, primarily the 2.4 GHz band and the 5.2 GHz band. Devices must have separate RF (Radio Frequency) hardware for the two frequency bands to enable dual band WLAN. The dual band Low Noise Amplifier (LNA) is used in this case. The LNA is a critical component in the RF front end of WLAN devices, as it amplifies the weak incoming signals from the antennas while maintaining low noise levels [1-3].

A dual band LNA is specifically designed to operate in two distinct frequency bands. This means it can amplify signals from two different frequency ranges or bands. It must have appropriate performances to ensure optimal signal amplification with other parameters are comparable for both

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bands. Some key considerations in designing dual band LNAs for WLAN are gain, noise figure, linearity, power consumption, cost, and size [4]. One of the key challenges, as mentioned in [5,6],is establishing a balance between gain and noise figure within both frequency ranges. Another significant problem in LNA design is impedance matching. Several methods for matching the impedance of multiband LNAs have been presented in the literature [7-10]. Achieving optimal matching for both frequency bands can be complex, and mismatches may lead to signal reflections, reduced gain, and degraded overall performance. Besides, power dissipation is also becoming a crucial issue in most circuit design [11].

This paper presents a dual band low noise amplifier (LNA) implemented using 130 nm CMOS technology. It introduces the forward body bias technique that decrease the threshold voltages which leads to a low supply voltage, effectively reduces power consumption [12-14]. Additionally, the use of source degeneration inductor improves the noise figure [15,16]. The paper is structured with the design methodology discussed in Section 2, followed by the presentation of results in Section 3. Section 4 provides the simulation results. Finally, the conclusions are outlined in Section 5.

2. Design Methodology

Figure 1 shows the schematic of the proposed dual band LNA by using 130 nm CMOS technology. A positive bulk-source voltage is provided to both M_1 and M_2 to lower supply voltage implementing the forward body bias approach. The transistors are connected in cascode configuration which can improve the gain of the LNA.

The threshold voltage of a channel MOSFET is defined as [17]:

$$V_{th} = V_{tho} + \gamma\left(\left(\sqrt{2\emptyset_f - V_{bs}}\right) - \sqrt{2\emptyset_f}\right) \quad (1)$$

where Vbs is the body to source voltage, V_{tho} is the threshold voltage for V_{bs} = 0, γ is a process dependent parameter, and $\emptyset_f$ is a semiconductor parameter with a typical value in the 0.3-0.4 V range [17]. Based on the equation, boosting V_{bs} lowers V_{th}, which lowers power supply and power consumption [18-20]. As the MOSFET's source to body connection's forward body bias varies, a DC current flows across the junction with an exponential reliance on the body voltage, resulting in increased power consumption and perhaps latch up failure. A current limiting resistor, R_B, is connected to the body terminal to avoid excessive junction conduction. It might easily be determined that a large bias resistor results in minimal noise.

The cascode stages are built on a straightforward common source transistor. The common source architecture with source inductor degeneration enabled input impedance matching with noiseless devices, resulting in a low NF. For both bands, the LNA's input impedance should be near to 50 Ω. As a result, passive circuits are mostly used to provide both input matching and dual band operation at the same time. The cascade LNA is built with NMOS transistors to provide low power performance. To boost the gain of the LNA, the transistor sizes (W/L ratios) are raised and optimized. All transistors are biased to lower the supply voltage, V_{DD}, to 0.6 V.

R1 and RG2's function is to regulate the current flow from the DC voltages of VG1 and VG2. As a result, the current passing through each transistor will be at a minimum, and the transistor will be protected against excessive current. Meanwhile, the values of L_1 and C_1 for 2.4 GHz and L_2 and C_2 for 5.2 GHz influence input matching. The values of L_3, C_3, R_2, L_4, and C_4 define the output matching portion. The greater the value of R2, the lower the NF but the higher the gain. The common source architecture with source inductor degeneration, L_S produced input impedance matching with noiseless devices, resulting in a low NF [21].

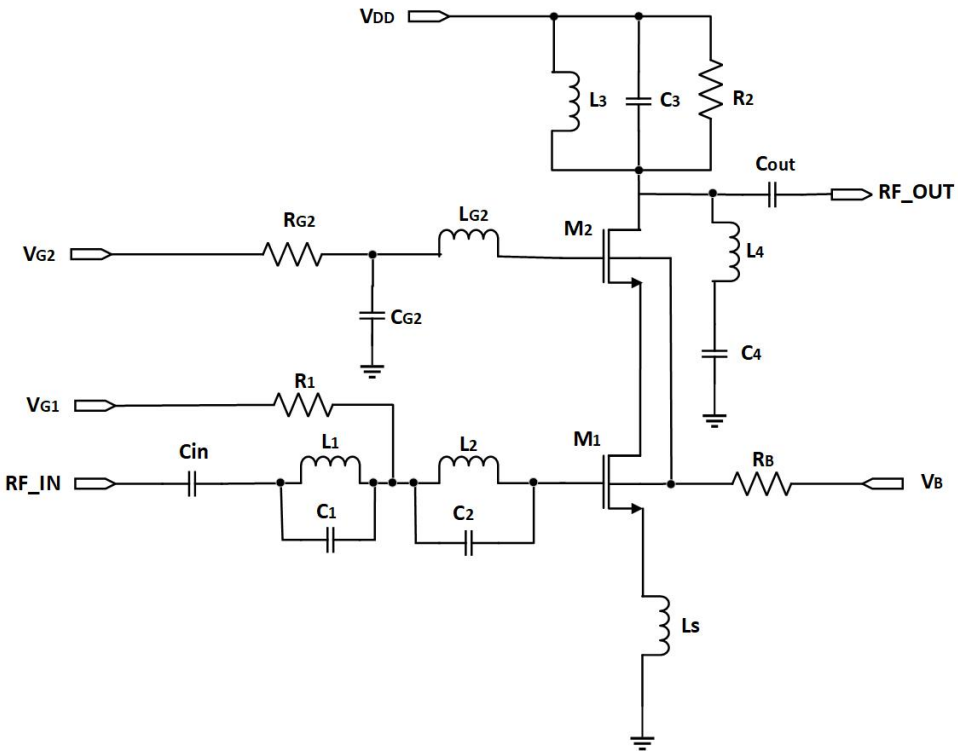

Fig. 1. The schematic of dual band LNA with forward body bias

3. Results

This section shows the results of the proposed dual band LNA design, which uses the forward body bias approach to lower the threshold voltage and hence reduce power consumption. Furthermore, at 2.4 and 5.2 GHz, the notch filter approach guarantees good input and output matching. The results of the post-layout simulation show that the dual band LNA achieves a low power consumption of 5.8 mW from a 0.6 V supply voltage while retaining acceptable parameters.

Figure 2 depicts the voltage gain (S21) of the dual band LNA's forward body bias with cascode variants. S21 is 16.1 dB at 2.4 GHz and 14.9 dB at 5.2 GHz, according to simulation data. However, parasitic effects, notably parasitic resistance in load inductors, have an influence on the circuit's gain.

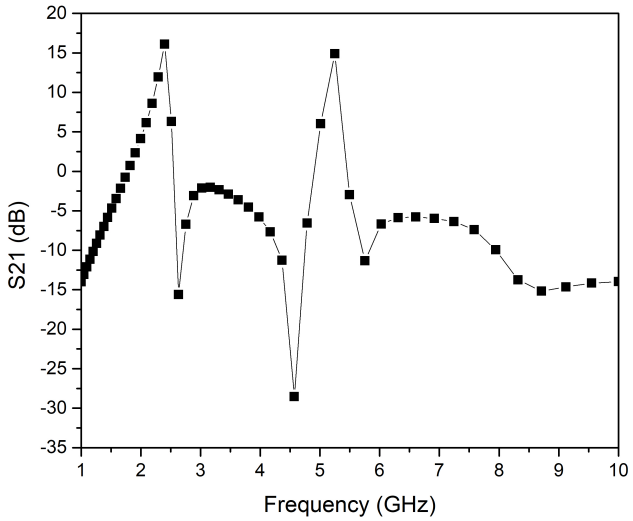

Fig. 2. Gain (S21) of the proposed dual band LNA

Figure 3 depicts the simulation results of the suggested LNA's input matching. The pre-layout input return loss (S11) at 2.4 GHz is -23.7 dB, whereas it is -14.9 dB at 5.2 GHz, which can be ascribed to parasitic effects such as inductor substrate parasitic and input capacitance. The input matching value, on the other hand, is judged acceptable and falls within the desired range. Figure 4 depicts the output matching of the proposed dual band LNA, displaying a simulated S22 at 2.4 GHz is -12.7 dB, whereas it is -10.2 dB at 5.2 GHz.

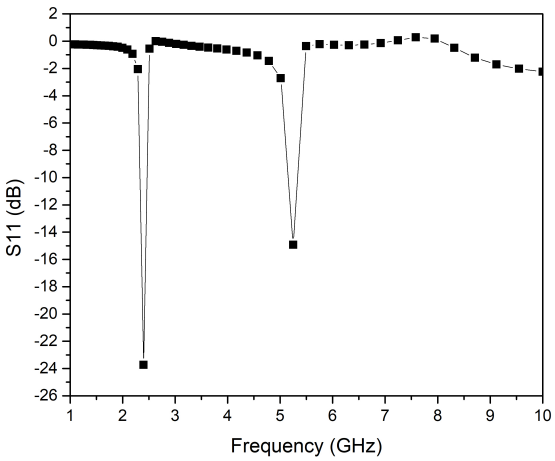

Fig. 3. Input return loss (S11) of the proposed dual band LNA

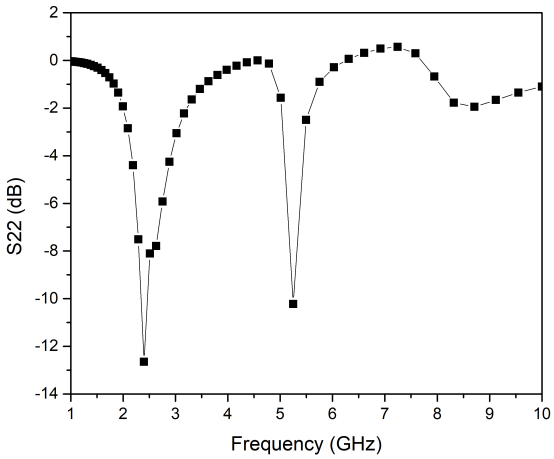

Fig. 4. Output return loss (S11) of the proposed dual band LNA

Figure 5 depicts the noise figure (NF) pre-layout findings. At 2.4 GHz and 5.2 GHz, the circuit obtains an NF of 2.7 dBm and 1.7 dBm, respectively. The curve of the stability factor is shown in Figure 6. The LNA is unconditionally stable, having stability values greater than one at both frequencies.

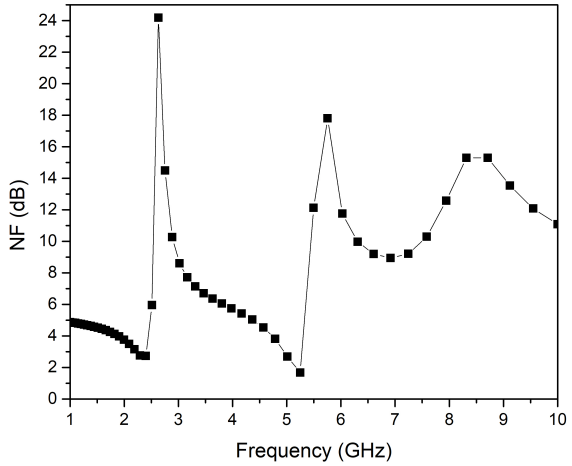

Fig. 5. Noise Figure (NF) of the proposed dual band LNA

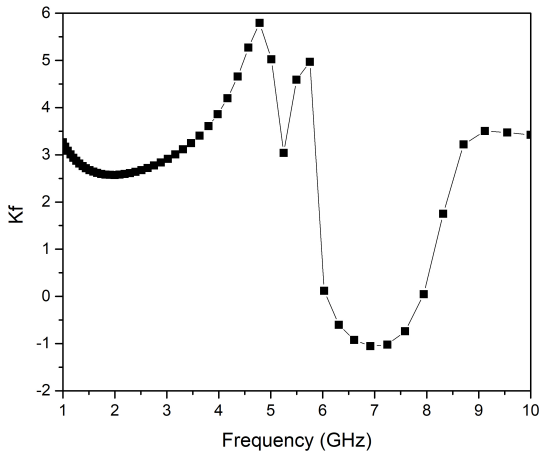

Fig. 6. Stability of the proposed dual band LNA

Table 1 shows a comparison between our study with previously reported dual band LNAs. To increase gain, a cascode arrangement with a capacitor and linked inductor was added to [2]. The cascode common source architecture was used in [3] to provide greater gain simultaneous and input matching at 2.4 and 5.2 GHz together with LC network band pass and band stop notch filters at the input and output stages. In [4], the resistive shunt feedback current reused structure is used to

decrease power dissipation, while the second inverter-based stage is utilised to boost gain. In [19], a common source stage with a current reused method was used to decrease power consumption. The frequency response of the proposed LNA is shaped by using notch filters at the input and output networks. Finally, in [20], a linearization approach was applied to improve the input third-order intercept point (IIP3) and an enhanced output matching network was built for wireless and Bluetooth applications utilising a 65 nm CMOS technology. This suggested dual band LNA produces a low noise figure compared to previous published work. Besides, by implementing forward body bias technique, a low supply voltage hence reduces power consumption but retaining equivalent other parameters.

Table 1
Performance comparison with previously published dual band LNA

Parameter	[1]*	[3]*	[4]*	[22]	[23]	This work
CMOS Technology(µm)	0.13	0.13	0.18	0.18	0.65	0.13
Frequency (GHz)	2.4	2.4	2.4	2.4	2.4	2.4
	5.2	5.2	5.2	5.2	5.2	5.2
Supply Voltage (V)	1.2	1.2	1.5	1.5	1.0	0.6
S21 (dB)	21.8	17.1	13.7	15.1	14.2	16.1
	14.2	8.5	14.1	13	11	14.9
S11 (dB)	-18	-15.6	-12.9	-13.3	-24.3	-23.7
	-16	-13.8	-14.6	-12.4	-26.4	-14.9
S22 (dB)	-14	N/A	N/A	N/A	N/A	-12.7
	-16	N/A	N/A	N/A	N/A	-10.2
IIP3 (dBm)	7	N/A	-6	-16	-1.66	-20
	10	N/A	-11	-10	0.04	-20
NF (dB)	4.1	3.6	4.2	2.7	2.4	2.7
	5.0	3.3	4.6	3.2	4.5	1.7
Power (mW)	32.9	9.8	10.8	2.5	3.6	5.8

* post layout simulation

4. Conclusions

In 130 nm CMOS Silterra Technology, a dual band 2.4 and 5.2 GHz low noise amplifier with low voltage and power consumption was presented. The input impedance in both frequency ranges was matched. The suggested LNA has gains of 16.1 dB and 14.9 dB, respectively, with input return losses of -23.7 dB and -14.9 dB at 2.4 GHz and 5.2 GHz. The noise value is 2.7 dBm at 2.4 GHz and 1.7 dBm at 5.2 GHz, respectively. Using forward body bias with cascode architecture, the supply voltage and power consumption were significantly decreased while the LNA gain was improved. Meanwhile, the noise figure performs better than previous works. When compared to earlier published publications, the LNA characteristics demonstrate improved performance in both frequency ranges as well as lower voltage and power consumption.

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