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Improved Domino Logic Based Low Power CMOS Schmitt Trigger Circuit at Nano Scale Regime

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ABSTRACT

The requirement of high-speed low power square wave generators that yield spike free signal enabled the design of Schmitt trigger circuit. The designs BJT or FET based circuits have disadvantages like spikes in output signal cannot be suppressed, the output signal gain control is required, low packing density, considerable power dissipation, etc. This has paved way to development of CMOS based design. As the technology scales down, the CMOS logic undergoes power dissipation due to high packing density caused by dominant leakage currents. Hence, low power requirement enabled the CMOS based low power design aspects for the Schmitt trigger circuit. The designs are modeled in DSCH and Microwind Tools for schematic and layout development at various technologies like 90 nm, 65 nm, 45 nm and 32 nm and the designs are evaluated from HSPICE Tool. The choice of designs used are conventional domino logic, clock delayed domino keeper logic, clock delayed domino keeper logic with discharge path, foot driven stacked transistor logic, ground PMOS keeper logic, leakage current based logic, high speed domino logic and proposed clocked delayed dual keeper logic. The area is a trade-off parameter for proposed clocked delayed dual keeper design with an increase in area by at least 9.8%. However, the area occupied by conventional domino-based Schmitt trigger design is least due to usage of lesser number of transistors. The power dissipation is less for proposed clocked delayed dual keeper design by at least 3.27%. However, the power dissipation is least for Leakage Current based Schmitt trigger design due to usage of lesser number of transistors.

Keywords:

Domino logic; leakage current; power consumption; robustness; Schmitt trigger

1. Introduction

The wave generated from signal inverter provides the signal in opposite to that of the input signal which reacts to changes in input logic levels as shown in Figure 1, such as spikes, hazards, etc. To overcome this, CMOS Schmitt trigger circuit is used to generate square waveform as taken from the previous studies [1]. The Schmitt Trigger circuits are used to suppress the noise in output signals for signal conditioning applications used in digital circuits that are generated from

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mechanical contact bounce in switches. Hence it is used as a function generator that is capable of converting Sine and Triangular Wave Inputs to Square Wave Outputs.

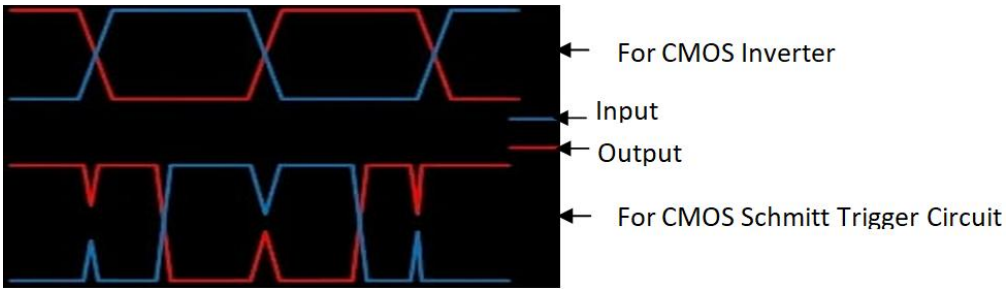
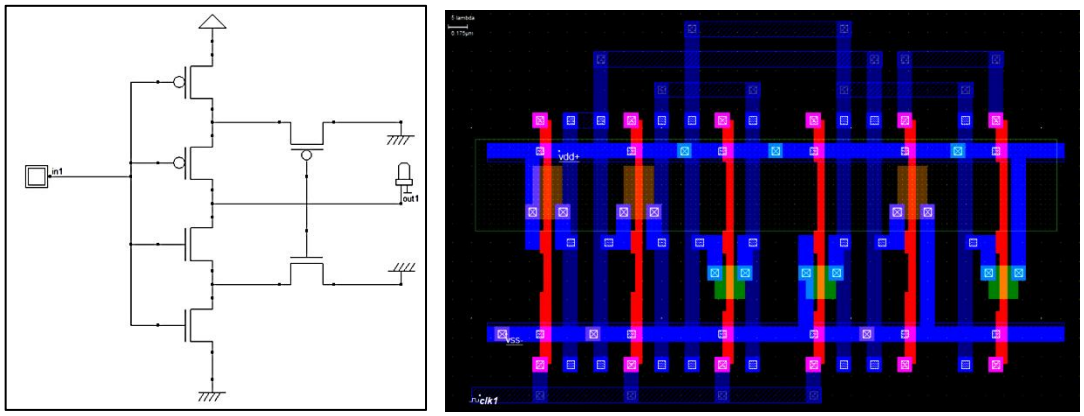


Fig. 1. Signal inverter circuit response

The Schmitt trigger circuits are used to suppress the noise in output signals for signal conditioning applications used in digital circuits that are generated from mechanical contact bounce in switches. Hence it is used as a function generator that is capable of converting Sine and Triangular Wave Inputs to Square Wave Outputs. In Figure 1, the first set of signals is represented for normal CMOS inverter, where the blue color represents the input and red color represents the output. This signal can be obtained only if proper pull up and pull-down ratios of the respective PMOS and NMOS transistors are used. For CMOS based Schmitt trigger based circuit, the spikes in circuit input and output response can be clearly observed.

The basic circuit uses two series PMOS in Pull-Up Network (PUN) and two series NMOS in Pull-Down Network (PDN) along with a set of pass transistors i.e., a PMOS and a NMOS are used in positive feedback to the circuit as shown in Figure 2(a) as a schematic diagram developed in DSCH Tool. When the Vin is logic LOW, the PUN is turned ON causing the Vout equating to VDD. When Vin is logic HIGH, then the PDN consisting of two NMOS transistors turns ON, which make Vout to logic LOW. The Figure 2(b) shows the corresponding layout developed in Microwind Tool at 90nm technology as taken from the previous studies [2, 3].



(a) (b)

Fig. 2. Basic CMOS Schmitt trigger circuit (a) Schematic diagram (b) Layout diagram

The features include the static power dissipation as taken from the previous studies [4, 5] is zero as there is no short between ground and VDD and the switching threshold depends on the transistor size as taken from the previous studies [6, 7]. This CMOS based Schmitt trigger circuit operates at low supply voltage i.e., from 0.8V to 1.5V with lesser propagation delay as taken from the previous studies [8-10].

In Future, the designs may be developed for new devices like CNTFETs, Quantum Dot Cellular Automata, etc. The multilevel logic can be used for ternary, quaternary logic, etc. The research for reducing the leakage power dissipation is aimed at reducing the leakage currents alone by using keeper gate. However, the research focus may also include the reduction of static and dynamic power dissipation.

2. Methodology

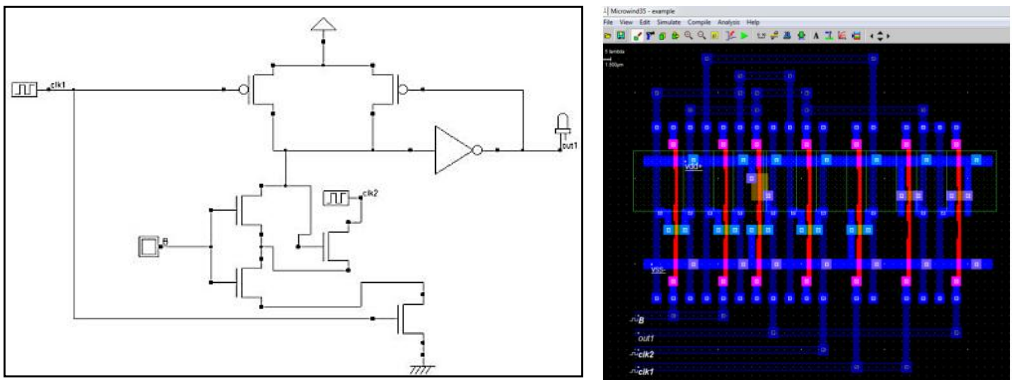
The various methods used to develop the low power circuits are discussed here. The low power techniques described here focus on reducing the dynamic power dissipation rather than the static and leakage power dissipation as taken from the previous studies [11-15]. Domino logic is one of the alternative logics for CMOS based low power designs that operate for non-inverting circuits. Hence a static CMOS inverter at the output remains a preliminary aspect in every possible design. In some cases, this static CMOS inverter can be used as a keeper circuit as taken from the previous studies [16-20].

2.1 Conventional Domino Based Schmitt Trigger Circuit

The PUN has a single PMOS transistor for precharge and PDN has NMOS transistors for evaluation, along with inverter connected to the dynamic node at output as taken from the previous studies [21-25] is implemented for Schmitt trigger as shown in Figure 3. The general applicability of the low power designs is verified for Schmitt trigger circuits and SRAM designs as taken from the previous studies [26-27]. This conventional Domino logic, when clock is low, output charges to VDD during precharge phase and keeps the keeper transistor ON and in evaluation phase clock is high, output depends on the inputs to remain at VDD or discharge to GND.

In spite of any noise, when all inputs are kept low, the keeper transistor will maintain the output at logic high. When any input turns high, the keeper transistor is turned off and output is discharged.For better noise margin, the keeper transistor width is maintained large. But the contention also increases making the gate to respond slowly. Hence the trade-off exist is for speed and noise margin, it is severe at lower Vts due to increased leakage of NMOS transistor.

The layout diagram as shown in Figure 3(b) shows the various input and output signals along with three PMOS and five NMOS transistors interconnected by metal layers, whose netlist matches with the schematic diagram shown in Figure 3(a). This layout is developed at 90nm in Microwind Tool.

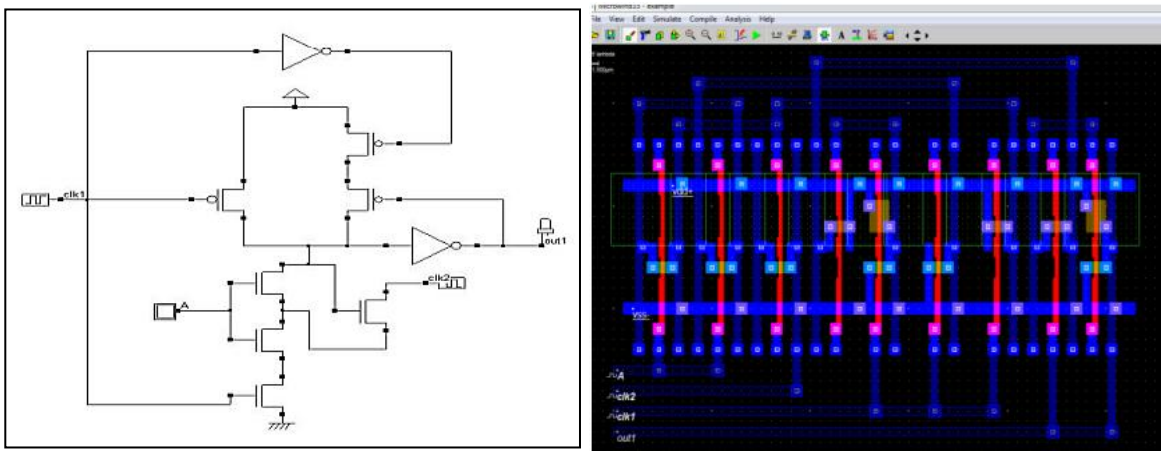


(a) (b)

Fig. 3. Conventional Domino based Schmitt trigger circuit (a) Schematic diagram (b) Layout diagram

2.2 Clocked Delayed Dual Keeper Based Schmitt Trigger Circuit

In CDDK Domino Circuit implemented for Schmitt trigger, the keeper circuit is modified to have series connection of two PMOS transistors delay the current to reduce contention during evaluation as shown in Figure 4. When clock is low, the output node is charged to VDD through keeper transistor. When clock is HIGH, the keeper transistor is disabled which delays the inverted clock for the gate. Hence the PDN discharges with high speed in accordance with the inputs. Here the drawback is in variations of the loop gain and its process that contributes to variations in delay. The layout diagram as shown in Figure 4(b) matches the netlist of the schematic diagram shown in Figure 4(a) for the available number of input and output signals along with five PMOS and six NMOS transistors interconnected by metal layers, developed at 90nm in Microwind Tool.



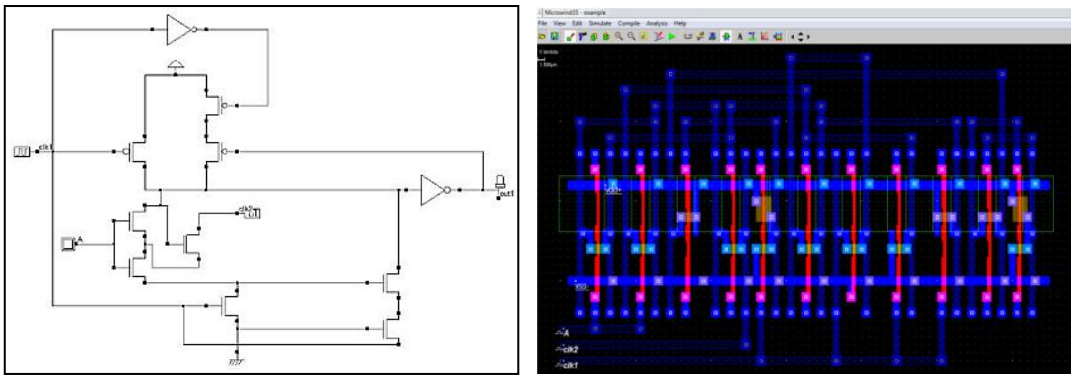
(a) (b)

Fig. 4. Clocked delayed dual keeper based Schmitt trigger circuit (a) Schematic diagram (b) Layout diagram

2.3 Clocked Delayed Domino Keeper Discharge Path Logic Based Schmitt Trigger Circuit

In this circuit, the keeper is enabled by delayed inverted clock signal. During precharge phasei.e., CLK = 0, the PUN transistors are turned ON which discharge the output node to GND. During evaluation phase, i.e., CLK = 1, the keeper transistor is turned OFF due to inverted delayed clock. The delay incurred in turning ON the keeper transistor is the propagation delay depends on inverter size which also reduces the contention current.

When PDN evaluates to VDD, the output node has to be fully discharged to enhance speed, during which the keeper remains cut-off. Hence, the speed can be enhanced by delaying the enabling of keeper circuit, controlling the swing variation of keeper circuit, sizing of keeper transistors and using a conditional discharge path. Further the implemented Schmitt trigger circuit robustness is taken care by upsized stacked dual keeper transistors is as shown in Figure 5. Still, variability in delay resides. The layout diagram as shown in Figure 5(b) matches the netlist of the schematic diagram shown in Figure 5(a) for the available number of input and output signals along with five PMOS and eight NMOS transistors interconnected by metal layers, developed at 90nm in Microwind Tool.



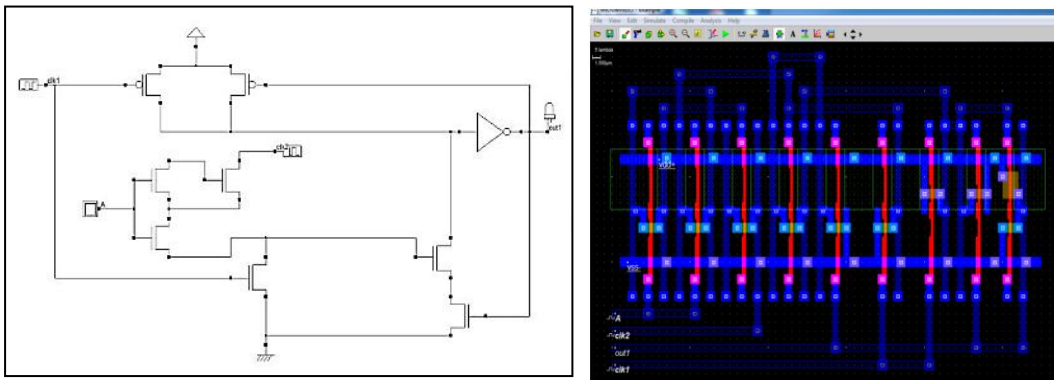
(a) (b)

Fig. 5. Clocked delayed Domino keeper discharge path logic based Schmitt trigger circuit (a) Schematic diagram (b) Layout diagram

2.4 Foot Driven Stacked Transistor Based Schmitt Trigger Circuit

In this Foot-Driven Stacked Transistor Domino Logic (FDSTDL) circuit implemented for Schmitt trigger, delay is reduced in discharge of dynamic node by adding an additional discharge path at the output to accelerate the transitions being controlled by output and foot node voltages as shown in Figure 6. A feedback from gate to current mirror and to output of the circuit is used to control dynamic discharge of output node. When output discharges to GND with noisy inputs, the stacked transistor connects mirror transistors input to ground. In evaluation phase, clock = 1 and all inputs are 0,then the stacked transistors decrease the subthreshold current which improves noise immunity. Still an increase in area is observed.

The layout diagram as shown in Figure 6(b) matches the netlist of the schematic diagram shown in Figure 6(a) for the available number of input and output signals along with three PMOS and seven NMOS transistors interconnected by metal layers, developed at 90nm in Microwind Tool.



(a) (b)

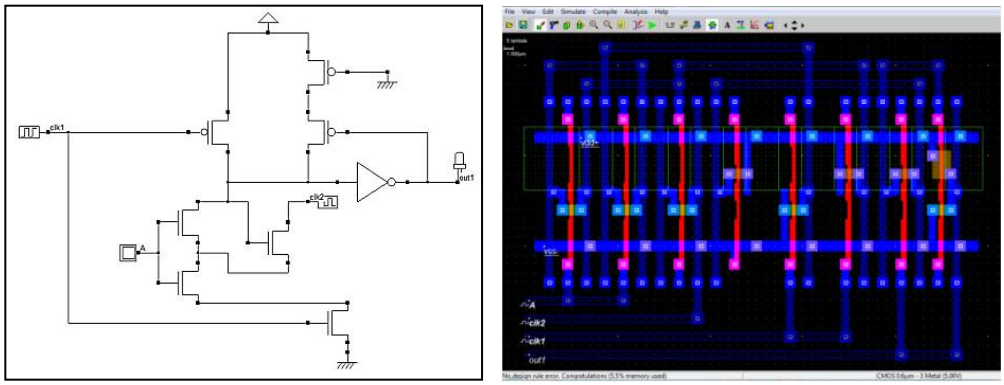
Fig. 6. Foot driven stacked transistor based Schmitt trigger circuit (a) Schematic diagram (b) Layout diagram

2.5 Ground PMOS Keeper Based Schmitt trigger circuit

In grounded PMOS keeper structure implemented for Schmitt trigger as shown in Figure 7, to reduce the loop gain and delay, an additional keeper PMOS transistor is used. The applications include digital circuits to prevent floating nodes causing unpredictable behavior with increased

power consumption. They can be used in various types of circuits, such as static random-access memory (SRAM) and register files, to ensure that the stored data remains stable when the circuit is not being actively driven. Ground PMOS keepers can also be used in power management circuits to keep unused logic blocks in a low-power state. Thus, grounded PMOS keeper solution is oriented towards power reduction, charge sharing prevention, increase in speed andmaintenance of robustness. The drawback is considerable power consumption as the PMOS transistor is always on and causes a voltage drop that affects the performance of the circuit.

The layout diagram as shown in Figure 7(b) is developed at 90nm technology in Microwind Tool, which matches the netlist of the schematic diagram shown in Figure 7(a) for the available number of input and output signals along with four PMOS and five NMOS transistors interconnected by metal layers.

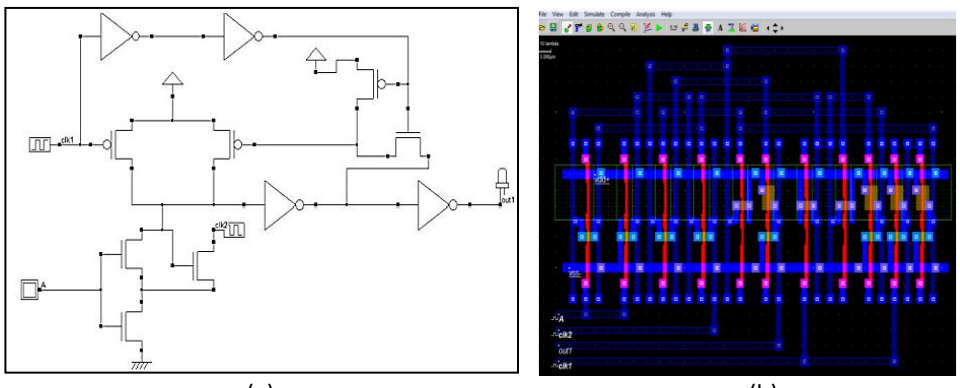


(a) (b)

Fig. 7. Ground PMOS keepers based Schmitt trigger circuit (a) Schematik diagram (b) Layout diagram

2.6 High Speed Domain Based Schmitt Trigger Circuit

In HSD Logic, the keeper control circuit is turned ON after a small delay that causes the output node to float as shown in Figure 8. During precharge, transistor is turned on causing output node to discharge. The delay is equal to that of two inverters by using sizing of transistors. In evaluation mode, the keeper transistor is biased which decreases leakage current and power. The speed of the logicvaries as per keeper transistors size. The layout diagram developed at 90 nm in Microwind Tool is as shown in Figure 8(b) matches the netlist of the schematic diagram shown in Figure 8(a) for the available number of input and output signals along with seven PMOS and eight NMOS transistors interconnected by metal layers.



(a) (b)

Fig. 8. High speed Domain based Schmitt trigger circuit (a) Schematic diagram (b) Layout diagram

2.7 Leakage Current Replica (LCR) Keeper Technique Based Schmitt Trigger Circuit

Leakage current is a composition of residual and subthreshold currents that flows through a transistor when it is supposed to be in the off state. It can be a significant power consumption source in digital circuits, particularly in high-density designs with many transistors. In Leakage Current Replica (LCR) Keeper circuit implemented for Schmitt trigger as shown in Figure 9, the analog current mirror circuit operated by leakage current of PDN controls the strength of the keeper transistor.

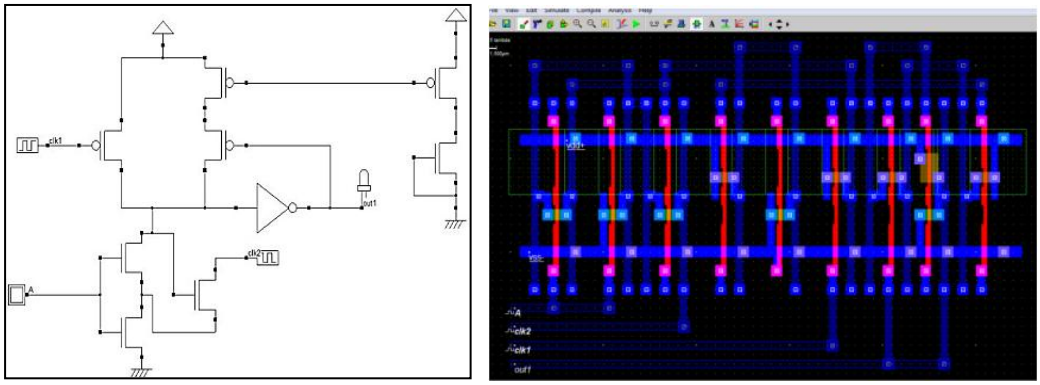
In domino logic, leakage transistors are used to prevent unwanted charge buildup in the recharged phase. During the recharge phase, the output is driven to a high voltage to prepare it for the evaluation phase. But, in evaluation phase, transistors may not be perfectly off, some charge may leak through and accumulate on the output node, causing incorrect logic behavior or increased power consumption.

To prevent this, a leakage transistor is added in parallel toevaluation transistor. The leakage transistor is sized to have a larger threshold voltage than the evaluation transistor, so it remains off during the recharge phase. In evaluation phase, both the evaluation and leakage transistors are turned on, allowing the circuit to operate normally.

The use of a leakage transistor can help to reduce power and improve performance of the domino logic circuit by preventing charge buildup and improving the accuracy of the logic operation. However, it can also add complexity to the design and increase area and power consumption. Therefore, it is important to carefully consider the trade-offs and optimize the design accordingly.

In domino logic, leakage transistors are used to prevent unwanted charge buildup in the recharged phase of the circuit. During the recharge phase, the output is driven to a high voltage to prepare it for the evaluation phase. But, if the evaluation transistor is not perfectly off, some charge may leak through and accumulate on the output node, causing incorrect logic behavior or increased power consumption. In wider fan in circuits, it reduces robustness and increases power dissipation.

The layout diagram developed at 90nm in Microwind Tool is as shown in Figure 9(b) matches the netlist of the schematic diagram shown in Figure 9(a) for the available number of input and output signals along with five PMOS and five NMOS transistors interconnected by metal layers.

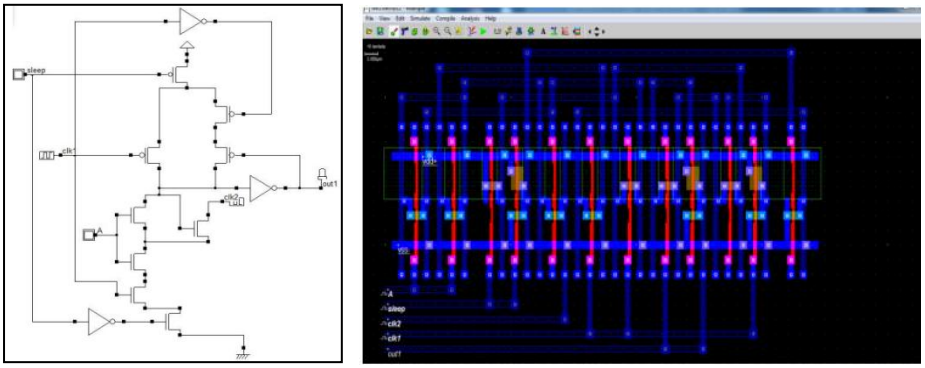


(a) (b)

Fig. 9. Leakage Current Replica (LCR) keeper technique based Schmitt trigger circuit (a) Schematic diagram (b) Layout diagram

2.8 Proposed Clock Delayed Dual Keeper Based Schmitt Trigger Circuit

Domino circuits are known for robust low power high-speed operation. This proposed circuit focuses on enhancing the speed of CDDK circuit as implemented for Schmitt trigger is as shown in Figure 10. This proposed CDDK technique uses two clocked delay stages in series to hold the precharged voltage level for a longer time to reduce the glitching effect. It can be used for other applications like microprocessors and memories, where performance and power efficiency are critical factors. The layout diagram developed at 90 nm in Microwind Tool is as shown in Figure 10(b) matches the netlist of the schematic diagram shown in Figure 10(a) for the available number of input and output signals along with seven PMOS and eight NMOS transistors interconnected by metal layers.



(a) (b)

Fig. 10. Proposed clock delayed dual keeper based Schmitt trigger circuit (a) Schematic diagram (b) Layout diagram

3. Results

The designs are developed in Digital Schematic for circuits and Microwind Tool for layouts at various nano scale technologies like 90 nm, 65 nm, 45 nm and 32 nm. The simulation waveform for Proposed clock delayed dual keeper based Schmitt trigger circuit is as shown in Figure 11. As expected, the required square waveform is obtained. Here C represents the clock signal, A represents the input signal, S represents the sleep signal, out represents the output signal and the remaining signal is intermediate output signal. The output response of the circuit depends purely on the clock and sleep signals as obtained from Figure 11. In the similar manner the simulation waveforms are obtained for other existing Schmitt trigger circuits.

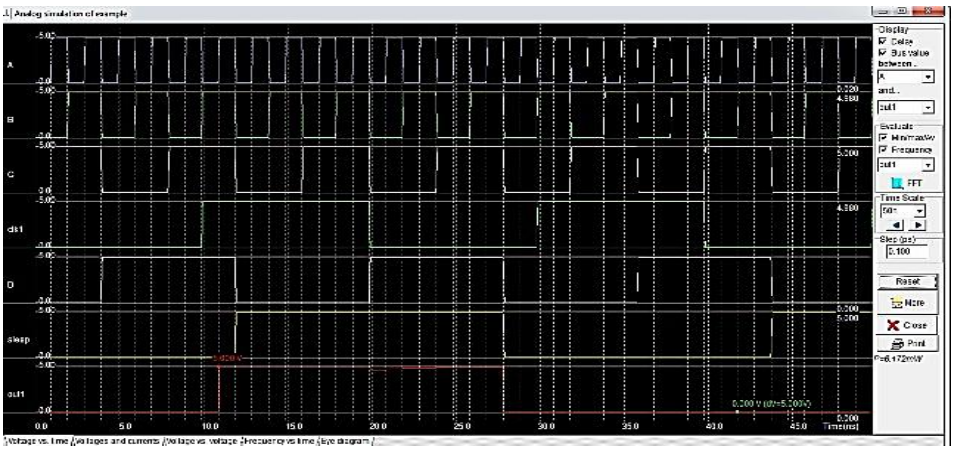
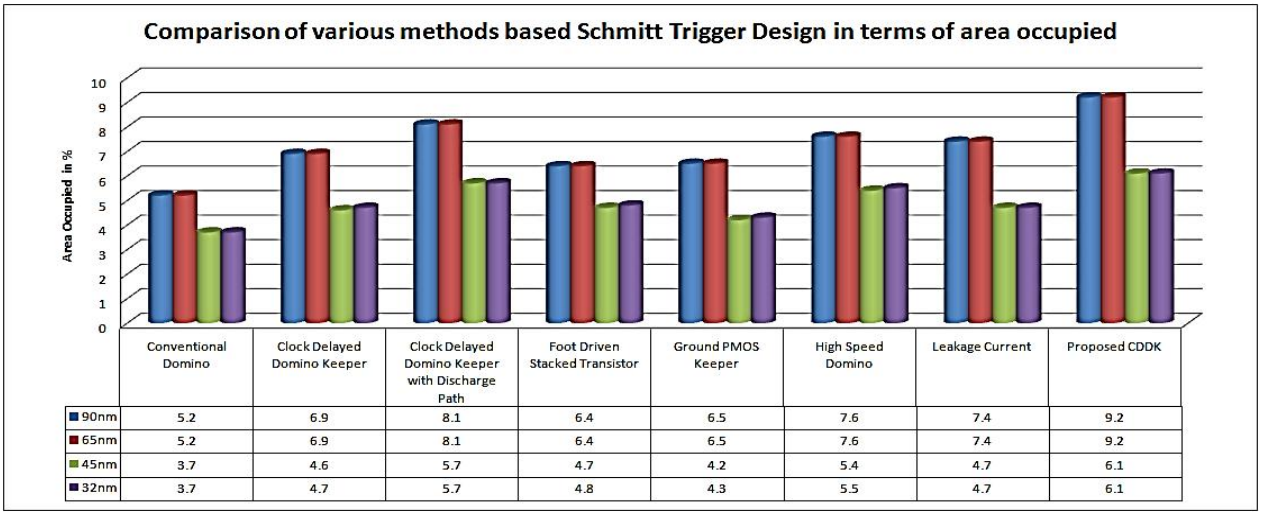


Fig. 11. Simulation waveform

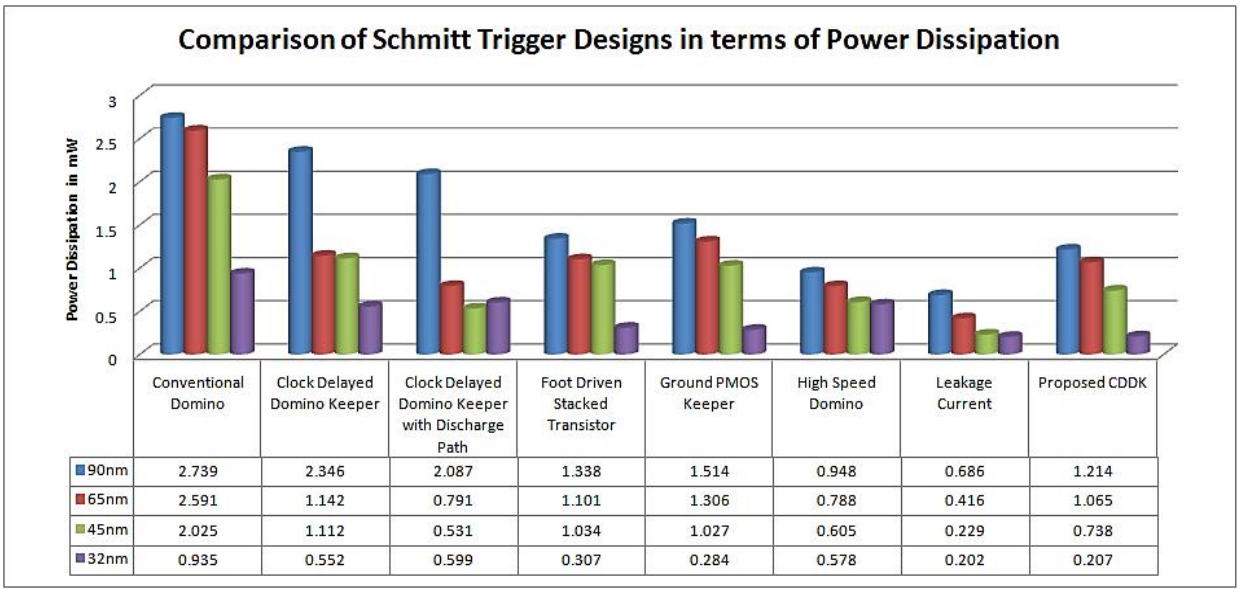
The designs are evaluated in HSPICE tool for area occupied and power dissipation as shown in Figures 12 and 13 respectively. From Figure 12, as the technology scales down, the designs occupy less area in terms of percentage in layout. For 90 nm to 65 nm technology, the proposed CDDK based Schmitt trigger design increases area by 43.47%, 25.00%, 11.95%, 30.43%, 29.34%, 17.39% and 19.56% when compared with the conventional domino, CDDK, CDDK with discharge path, foot driven stacked transistor, ground PMOS keeper, High speed domino and leakage current based existing Schmitt trigger designs respectively. For 45nm technology, the proposed CDDK based Schmitt trigger design increases area by 39.34%, 24.59%, 6.56%, 22.95%, 31.15%, 11.47% and 22.95% when compared with the conventional domino, CDDK, CDDK with discharge path, foot driven stacked transistor, ground PMOS keeper, High speed domino and leakage current based existing Schmitt trigger designs respectively.

For 32 nm technology, the proposed CDDK based Schmitt trigger design increases area by 39.34%, 22.95%, 6.56%, 21.31%, 29.51%, 9.84% and 22.95% when compared with the conventional domino, CDDK, CDDK with discharge path, foot driven stacked transistor, ground PMOS keeper, High speed domino and leakage current based existing Schmitt trigger Designs respectively. The area is a trade-off parameter for proposed CDDK design with an increase in area by atleast 9.8%. However the area occupied by conventional domino based Schmitt trigger design is least due to usage of lesser number of transistors.



	Conventional Domino	Clock Delayed Domino Keeper	Clock Delayed Domino Keeper with Discharge Path	Foot Driven Stacked Transistor	Ground PMOS Keeper	High Speed Domino	Leakage Current	Proposed CDDK
90nm	5.2	6.9	8.1	6.4	6.5	7.6	7.4	9.2
65nm	5.2	6.9	8.1	6.4	6.5	7.6	7.4	9.2
45nm	3.7	4.6	5.7	4.7	4.2	5.4	4.7	6.1
32nm	3.7	4.7	5.7	4.8	4.3	5.5	4.7	6.1

Fig. 12. Comparison of Schmitt trigger designs in terms of area occupied



	Conventional Domino	Clock Delayed Domino Keeper	Clock Delayed Domino Keeper with Discharge Path	Foot Driven Stacked Transistor	Ground PMOS Keeper	High Speed Domino	Leakage Current	Proposed CDDK
90nm	2.739	2.346	2.087	1.338	1.514	0.948	0.686	1.214
65nm	2.591	1.142	0.791	1.101	1.306	0.788	0.416	1.065
45nm	2.025	1.112	0.531	1.034	1.027	0.605	0.229	0.738
32nm	0.935	0.552	0.599	0.307	0.284	0.578	0.202	0.207

Fig. 13. Comparison of Schmitt trigger designs in terms of power dissipation

From Figure 13, as the technology scales down, the power dissipation for the designs is less due to reduced leakage power by keeper additional keeper transistors at physical level. For 90 nm technology, the proposed CDDK based Schmitt trigger design decreases power dissipation by 55.67%, 48.25%, 41.83%, 9.27%, 19.81%, but increased by 21.91% and 43.49% when compared with the conventional domino, CDDK, CDDK with discharge path, foot driven stacked transistor, ground PMOS keeper, High speed domino ad leakage current based existing Schmitt trigger designs respectively. For 65 nm technology, the proposed CDDK based Schmitt trigger design decreases power dissipation by 58.89%, 6.74%, -34.64%, 3.27%, 18.45%, but increased by 26.01% and 60.94% when compared with the conventional domino, CDDK, CDDK with discharge path, foot driven stacked transistor, ground PMOS keeper, High speed domino and leakage current based existing Schmitt trigger designs respectively.

For 45 nm technology, the proposed CDDK based Schmitt trigger design decreases power dissipation by 66.49%, 33.63%, increased by 38.98%, decreased by28.63%, 28.14%, but increased by18.02% and 68.97% when compared with the conventional domino, CDDK, CDDK with discharge path, foot driven stacked transistor, ground PMOS keeper, High speed domino and leakage current based existing Schmitt trigger designs respectively. For 32 nm technology, the proposed CDDK based Schmitt trigger design decreases power dissipation by 77.86%, 62.5%, 65.44%, 32.57%, 46.09%, 64.18% and increased by 2.41% when compared with the conventional domino, CDDK, CDDK with discharge path, foot driven stacked transistor, ground PMOS keeper, High speed domino and leakage current based existing Schmitt trigger designs respectively. Here negative sign indicates increase in power dissipation.

The power dissipation is less for proposed CDDK design by atleast 3.27%. However the power dissipation is least for leakage current based Schmitt trigger design due to usage of lesser number of transistors.

4. Conclusions

This paper satisfies the requirement of high-speed low power square wave generators that yield spike free signal enabled the design of Schmitt trigger circuit using various domino logic based low power methods. The designs are modeled in DSCH and Microwind Tools for schematic and layout development at various technologies like 90 nm, 65 nm, 45 nm and 32 nm and the results are

evaluated from HSPICE tool. The choice of designs used are conventional domino logic, clock delayed domino keeper logic, clock delayed domino keeper logic with discharge path, foot driven stacked transistor logic, ground PMOS keeper logic, leakage current based logic, high speed domino logic and proposed CDDK logic. The area is a trade-off parameter for proposed CDDK design with an increase in area by atleast 9.8%. However, the area occupied by conventional Domino-based Schmitt trigger design is least due to usage of lesser number of transistors. The power dissipation is less for proposed CDDK design by atleast 3.27%. However, the power dissipation is least for leakage current based Schmitt trigger design due to usage of lesser number of transistors.

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References

[1] Angeline, A. Anita, and VS Kanchana Bhaaskaran. "Speed enhancement techniques for clock-delayed dual keeper domino logic style." *International Journal of Electronics* 107, no. 8 (2020): 1239-1253. https://doi.org/10.1080/00207217.2020.1726486

[2] Saranya, N. Naga, V. Jean Shilpa, K. Jayakumar, P. Senthil, and M. Arun. "Novel slumped SRAM configuration using QCA leveraging differential voltage sensing for enhanced stability and efficiency." *Journal of Cybersecurity and Information Management* 1 (2024): 207-07. https://doi.org/10.54216/JCIM.140114

[3] Basha, Shaik Javid, and P. Venkatramana. "Analysis of crosstalk effects for ternary logic MWCNT bundled through silicon vias." *ECS Journal of Solid State Science and Technology* 12, no. 2 (2023): 021008. https://doi.org10.1149/2162-8777/acbbe9

[4] Begum, A. Yasmine, M. Balaji, and V. Satyanarayana. "Quantum dot cellular automata using a one-bit comparator for QCA gates." *Materials Today: Proceedings* 66 (2022): 3539-3546. https://doi.org/10.1016/j.matpr.2022.06.416

[5] Neelima K., M. Bharathi. "Gated-VDD based single ended SRAM arrays." *i-Manager's Journal on Circuits and Systems* 3, no. 2 (2015): 12-18. https://doi.org/10.26634/jcir.3.2.3411

[6] Neelima, K., and Purushotham Prasad Kalisetti. "Design of a low power and highly stable single ended SRAM cell." *i-Manager's Journal on Circuits & Systems* 3, no. 1 (2014): 28. https://doi.org/10.26634/jcir.3.1.3260

[7] Vobulapuram, Ramesh Kumar, Javid Basha Shaik, Venkatramana P, Durga Prasad Mekala, and Ujwala Lingayath. "Design of bilayer graphene nanoribbon tunnel field effect transistor." *Circuit World* 49, no. 2 (2023): 174-179. https://doi.org/10.1108/CW-05-2020-0079

[8] Cerqueira, Joao P., Jieyu Li, Jiangyi Li, Weifeng He, and Mingoo Seok. "A femto/pico-watt feedforward leakage self-suppression logic family in 180 nm to 28 nm technologies." In *2019 IEEE 62nd International Midwest Symposium on Circuits and Systems (MWSCAS)*, p. 1049-1052. IEEE, 2019. https://doi.org/10.1109/MWSCAS.2019.8885086

[9] Neelima, K., and KC Lakshmi Narayana. "Design of a novel gated 5T SRAM cell with low power dissipation in active and sleep mode." *i-Manager's Journal on Circuits & Systems* 2, no. 4 (2014): 13. https://doi.org/10.26634/jcir.2.4.3220

[10] Alioto, Massimo, Gaetano Palumbo, and Melita Pennisi. "Understanding the effect of process variations on the delay of static and domino logic." *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 18, no. 5 (2009): 697-710. https://doi.org/10.1109/TVLSI.2009.2015455

[11] Alvandpour, Atila, Ram K. Krishnamurthy, Krishnamurthy Soumyanath, and Shekhar Y. Borkar. "A sub-130-nm conditional keeper technique." *IEEE journal of solid-state circuits* 37, no. 5 (2002): 633-638. https://doi.org/10.1109/4.997857

[12] Anis, Mohab H., Mohamed W. Allam, and Mohamed I. Elmasry. "Energy-efficient noise-tolerant dynamic styles for scaled-down CMOS and MTCMOS technologies." *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 10, no. 2 (2002): 71-78. https://doi.org/10.1109/92.994977

[13] Peiravi, Ali, and Mohammad Asyaei. "Robust low leakage controlled keeper by current-comparison domino for wide fan-in gates." *Integration* 45, no. 1 (2012): 22-32. https://doi.org/10.1016/j.vlsi.2011.07.002
[14] Peiravi, Ali, and Mohammad Asyaei. "Current-comparison-based domino: New low-leakage high-speed domino circuit for wide fan-in gates." *IEEE transactions on very large scale integration (VLSI) systems* 21, no. 5 (2012): 934-943. https://doi.org/10.1109/TVLSI.2012.2202408
[15] Jeyasingh, Rakesh Gnana David, Navakanta Bhat, and Bharadwaj Amrutur. "Adaptive keeper design for dynamic logic circuits using rate sensing technique." *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 19, no. 2 (2009): 295-304. https://doi.org/10.1109/TVLSI.2009.2031650
[16] Anita Angeline, A., and V. S. Kanchana Bhaaskaran. "High performance domino logic circuit design by contention reduction." In *VLSI Design: Circuits, Systems and Applications: Select Proceedings of ICNETS2,* p. 161-168. Springer Singapore, 2018. https://doi.org/10.1007/978-981-10-7251-2_18
[17] Katrue, Srikanth, and Dhireesha Kudithipudi. "GALEOR: Leakage reduction for CMOS circuits." In *2008 15th IEEE International Conference on Electronics, Circuits and Systems*, pp. 574-577. IEEE, 2008. https://doi.org/10.1109/ICECS.2008.4674918
[18] Hanchate, Narender, and Nagarajan Ranganathan. "LECTOR: a technique for leakage reduction in CMOS circuits." *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 12, no. 2 (2004): 196-205. https://doi.org/10.1109/TVLSI.2003.821547
[19] El-Feky, Nagham Gamal, Dina Mohamed Ellaithy, and Mostafa Hassan Fedawy. "Ultra-wideband CMOS power amplifier for wireless body area network applications: a review." *International Journal of Electrical & Computer Engineering (2088-8708)* 13, no. 3 (2023). https://doi.org/10.11591/ijece.v13i3.pp2618-2631
[20] Al-Kofahi, Idrees S., Zaid Albataineh, and Ahmad Dagamseh. "A two-stage power amplifier design for ultra-wideband applications." *Int. J. Electr. Comput. Eng.(IJECE)* 11 (2021): 772-779. https://doi.org/10.11591/ijece.v11i1.pp772-779
[21] Raheem, Mohammed Abdul, and K. Manjunathachari. "A two channel analog front end design AFE design with continuous time rA modulator for ECG signal." *Int. J. Electr. Comput. Eng* 8 (2018): 5041. https://doi.org/10.11591/ijece.v8i6.pp5041-5049
[22] Chavan, Arunkumar Pundalik, and Ravish Aradhya. "Design of 5.1 GHz ultra-low power and wide tuning range hybrid oscillator." *International Journal of Electrical and Computer Engineering (IJECE)* 13, no. 4 (2023): 3778-3787. https://doi.org/10.11591/ijece.v13i4.pp3778-3787
[23] Keote, Minal, and P. T. Karule. "Design and implementation of low power multiplier using proposed two phase clocked adiabatic static CMOS logic circuit." *International Journal of Electrical and Computer Engineering* 8, no. 6 (2018): 4959. https://doi.org/10.11591/ijece.v8i6.pp4959-4971
[24] Khatak, Anil, Manoj Kumar, and Sanjeev Dhull. "Analysis of CMOS comparator in 90 nm technology with different power reduction techniques." *International Journal of Electrical and Computer Engineering* 8, no. 6 (2018): 4922. https://doi.org/10.11591/ijece.v8i6.pp4922-4931
[25] Almalkawi, Islam T., Ashraf H. Al-Bqerat, Awni Itradat, and Jamal N. Al-Karaki. "An efficient design of 45-nm CMOS low-noise charge sensitive amplifier for wireless receivers." *International Journal of Electrical and Computer Engineering (IJECE)* 12, no. 2 (2022): 1274-1285. 10. https://doi.org/11591/ijece.v12i2.pp1274-1285
[26] Maniteja, Nagella, Kota Sahithi, K. Neelima, and Kumar Raja Meruva. "Design and evaluation of low power CMOS based Schmitt trigger circuits." *Russian Microelectronics* 52, no. 6 (2023): 556-564. https://doi.org/10.1134/S1063739723700671
[27] Issa, Hanady H., Mahmoud S. Badran, Saleh M. Eisa, and Hani F. Ragai. "Low power 7 nm FinFET based 6T-SRAM design." *Journal of Advanced Research in Applied Mechanics* 42, no. 1 (2018): 12-17.