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Design of Concurrent Dual Band Low Noise Amplifier for WLAN Applications

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Dual band; low noise amplifier; forward body bias; WLAN

ABSTRACT

This paper presents a dual band LNA CMOS designed for a Wireless Local Area Network (WLAN) application using CMOS 0.13-µm Silterra technology. The proposed design incorporates forward body bias technique with cascode and notch filter configuration to achieve both low power consumption and high gain. The simulation results demonstrate a total power consumption of 2.39 mW at a low supply voltage of 0.5 V, with a gain of 16 dB at 2.4 GHz and 12 dB at 5.2 GHz. Additionally, input return loss of -12.3 dB and -14.2 dB with noise figures of 2.93 dBm and 4.23 dBm were obtained at 2.4 GHz and 5.2 GHz, respectively. Overall, this research contributes to the development of dual band LNA designs for WLAN applications.

1. Introduction

Wireless local area networks (WLANs) have seen significant growth and the demand for high-performance wireless devices has increased over the past few years. The design of a low noise amplifier (LNA) is critical to the overall operation of a WLAN system [1, 2]. Dual-band LNAs are useful in reducing the complexity and cost of WLAN systems while providing high-performance. These LNAs can operate at two frequency bands simultaneously and are particularly useful in WLAN applications that operate at different frequency bands, such as 2.4 GHz and 5.2 GHz.

The design of concurrent dual band low noise amplifiers (LNAs) is becoming increasingly important for modern wireless communication systems that require support for multiple frequency bands. However, designing a concurrent dual band LNA with good performance at both bands is a challenging task due to the conflicting design requirements of the two frequency bands. According to the study by [3, 4] one of the main challenges is achieving a good tradeoff between gain and noise figure in both frequency bands. Another challenge is minimizing the impact of process

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variations, which can lead to significant performance degradation in dual-band LNAs [5-7]. Recent design approaches have focused on improving the performance of dual-band LNAs while maintaining a compact circuit size and low fabrication cost. To achieve these goals, various circuit topologies and techniques have been proposed, including notch filter [8, 9], current-reuse [10, 11] and tunable matching networks [12, 13]. Despite the progress made in recent years, there are still several challenges that need to be addressed in the design of concurrent dual band LNAs. These include ensuring robustness against interference and signal distortion [2, 14] and achieving high linearity in both frequency bands [12, 15]. Furthermore, power dissipation has become a critical concern in most circuit design [16].

The goal of this study is to increase LNA performance and minimize power consumption by designing a concurrent dual band CMOS LNA at 2.4 GHz and 5.2 GHz utilizing forward body bias and the notch filter approach.

2. Design Methodology

The proposed schematic design is illustrated in Figure 1. The design implementation is based on the forward body bias architecture, which ensures low power consumption through the ability of transistors to turn on at low supply voltage [17, 18]. Moreover, this technique is cost effective and straightforward. The proposed dual band LNA incorporates a cascode configuration as to enhance the gain [19, 20]. M1 is connected in a common source configuration by grounding the source, while the gate of M1 serves as the input port, and the drain of M2 is the output port for signals. Low power consumption is ensured by immediately lowering the threshold voltage (Vth) of NMOS transistors when the body terminal is connected to a voltage source.

The proposed LNA design implementation incorporates a biasing voltage (VB) of 0.3 V, significantly lower than the PN junction turn-on voltage of 0.7 V, resulting in negligible leakage current in the NMOS transistor's body-source junction. Figure 1 shows that R1 and RG2 are the biasing resistances of transistors M1 and M2 gates, respectively, while R2 is connected to L2 and C2 for input matching. The values of L3, C3, R3, L4 and C4 define output matching at 2.4 GHz and 5.2 GHz.

Transistor size is a key factor when trying to achieve low power consumption while maximizing gain and efficiency. The design implementation involves setting the size of the transistors to achieve optimal current consumption and acceptable gain. To guarantee adequate linearity and efficiency, the sizes of MI and M2 are adjusted to 100 µm/0.13 µm and 300 µm/0.13 µm, with 10 and 30 fingers, respectively. Additionally, the output matching is achieved through the notch filter technique in which parallel RLC circuit of R3, C3, and L3 and series LC circuit of C4 and L4 which are tuned to match the desired values at center frequencies of 2.4 GHz and 5.2 GHz.

The small signal model illustrated in Figure 2 was employed to determine the input matching of the dual band LNA under consideration. The input impedance calculation are as follows.

$$Z_{in} = Z_{CGS1} + \left(R_2 \| \quad Z_{L2} \| \quad Z_{C2}\right) + \left(R_1 \| \quad \left(\left(Z_{L1} \| \quad Z_{C1}\right) + Z_{Cin}\right)\right) \tag{1}$$

$$Z_{in} = \frac{1}{jwCGS1} + \left(R_2 \| \quad \text{jwL2} \| \quad \frac{1}{jwC2}\right) + \left(R_1 \| \quad \left(\left(jwL1 \| \quad \frac{1}{jwC1}\right) + \frac{1}{jwCin}\right)\right) \tag{2}$$

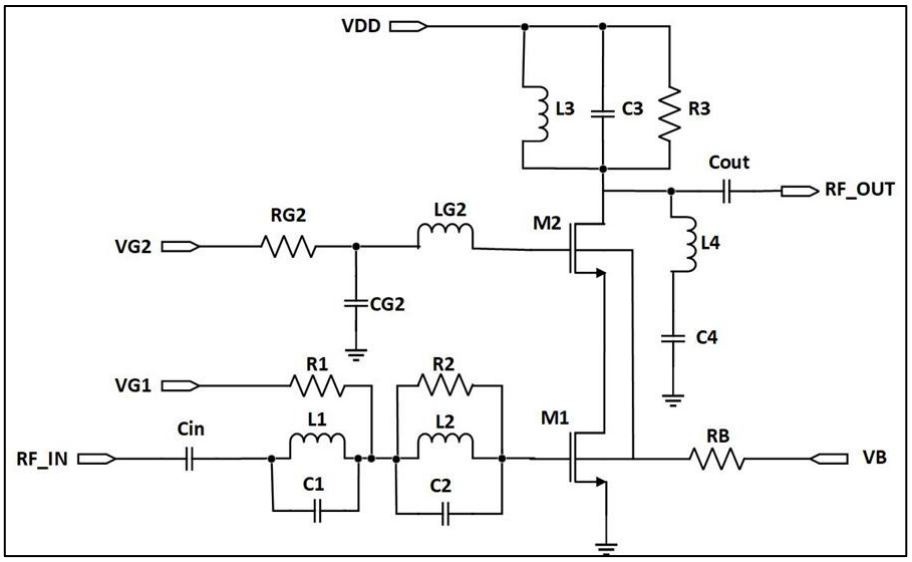

Fig. 1. The proposed schematic of dual band LNA for 2.4 GHz and 5.2 GHz

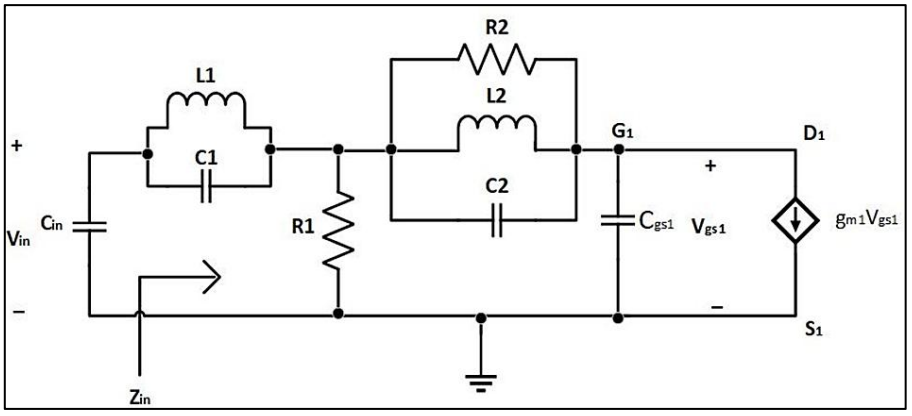

Fig. 2. A small signal model for calculating input impedance

Additionally, the output matching network of the LNA was depicted in Figure 3, which comprises a series connection of bandpass and band stop filter networks. The inductor and capacitor circuits were resonating at the intended operating frequencies of 2.4 GHz and 5.2 GHz. Consequently, the output impedance for this design can be expressed as a function of the input matching and LC components.

$$Z_O = Z_{L3} \| \quad Z_{C3} \| \quad Z_{R3} + Z_{L4} + Z_{C4} \tag{3}$$

$$Z_O = \left(jwL3 \| \quad \frac{1}{jwC3} \| \quad \mathrm{R3}\right) + jwL4 + \frac{1}{jwC4} \tag{4}$$

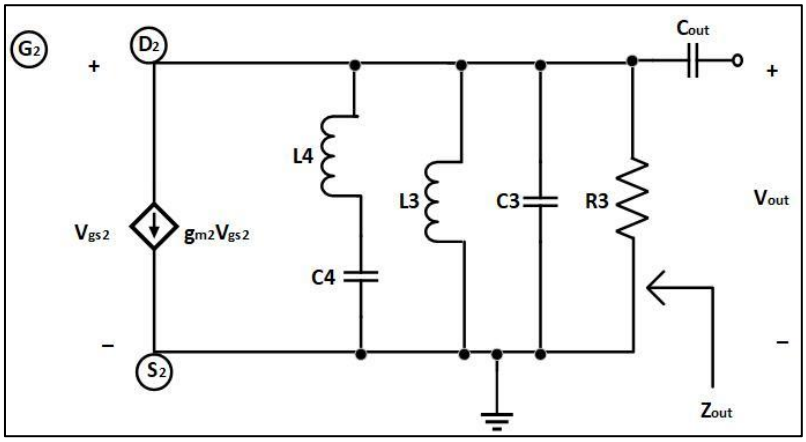

Fig. 3. A small signal model for calculating output impedance

3. Results

This section shows the results of the suggested dual band LNA design, which uses the forward body bias approach to minimize the threshold voltage and, as a result, power consumption. Furthermore, at 2.4 and 5.2 GHz, the notch filter approach guarantees good input and output matching. The results of the post-layout simulation show that the dual band LNA achieves a low power consumption of 2.39 mW from a 0.5 V power source while retaining acceptable parameters.

Figure 4 depicts the voltage gain (S21) of the dual-band LNA's forward body bias with cascode variants. According to simulation results, S21 is 15.76 dB at 2.4 GHz and 11.67 dB at 5.2 GHz. However, parasitic effects, notably parasitic resistance in load inductors, have an influence on the circuit's gain. Figure 5 depicts the simulation results of the suggested LNA's input matching. The pre-layout input return loss (S11) at 2.4 GHz is -12.3 dB, whereas it is -14.2 dB at 5.2 GHz, which can be ascribed to parasitic effects such as inductor-substrate parasitic and input capacitance. The input matching value, on the other hand, is judged acceptable and falls within the desired range. Figure 6 depicts the output matching of the proposed dual band LNA. Figure 6 shows the output matching of the proposed dual-band LNA, which reveals a simulated S22 of -14.37 dB at 2.4 GHz and -11.2 dB at 5.2 GHz.

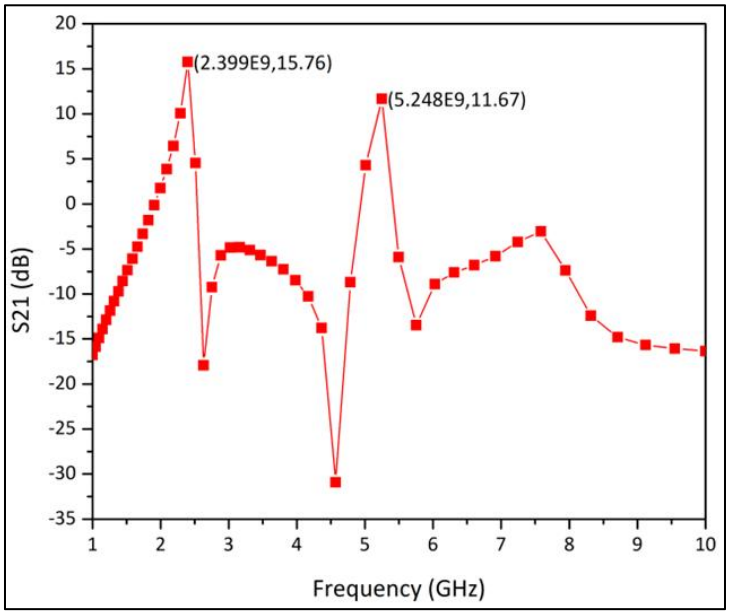

Fig. 4. Gain (S21) of the proposed dual band LNA

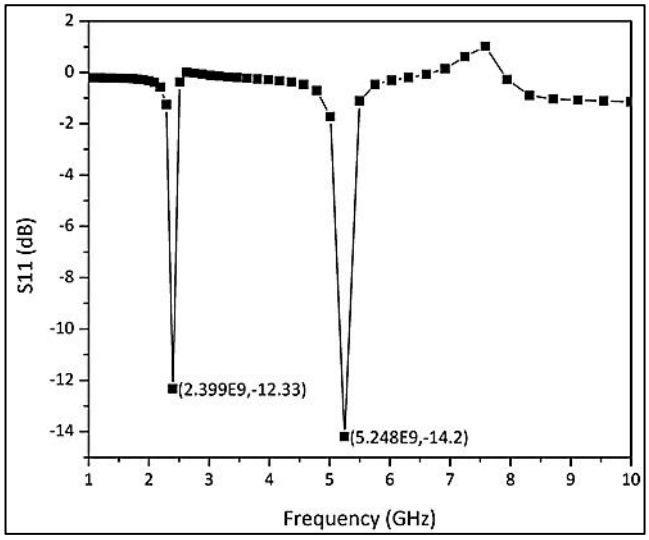

Fig. 5. Input return loss (S11) of the proposed dual band LNA

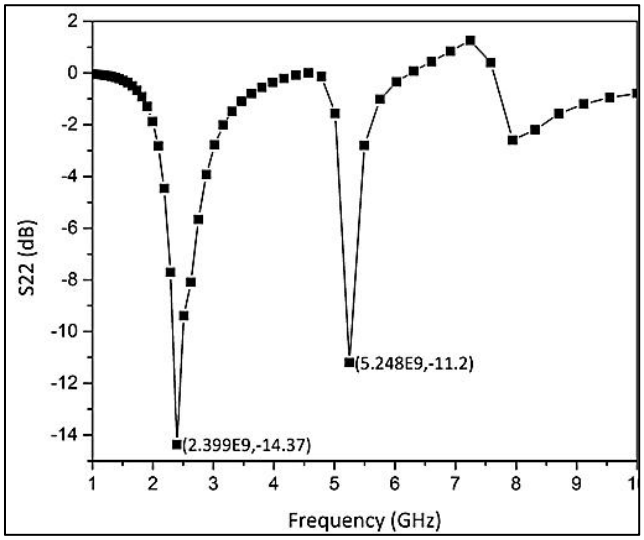

Fig. 6. Output return loss (S22) of the proposed dual band LNA

The pre-layout results for noise figure are depicted in Figure 7. The circuit achieves an NF of 2.97 dB and 4.22 dB at 2.4 GHz and 5.2 GHz, respectively. While the achieved NF is within specification, there is room for optimization. Figure 8 illustrates the stability factor plot. The LNA remains unconditionally stable, with stability values exceeding 1 for both frequencies.

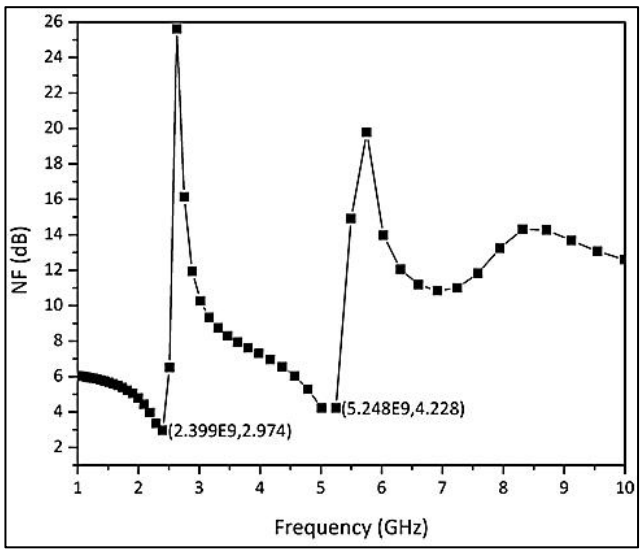

Fig. 7. Noise figure (NF) of the proposed dual band LNA

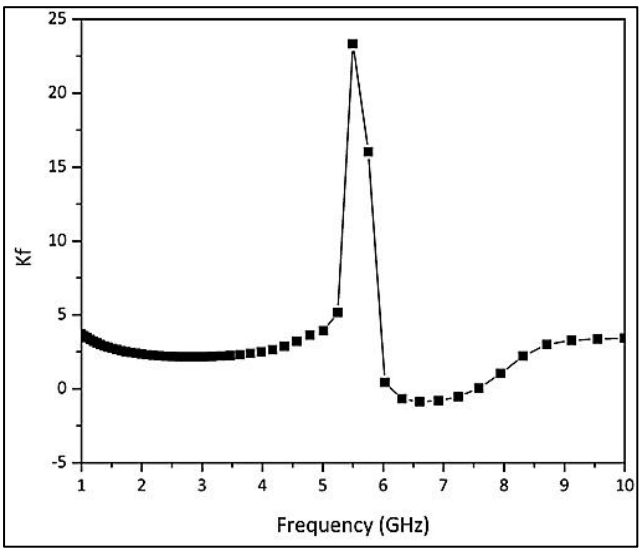

Fig. 8. Stability of the proposed dual band LNA

Table 1 compares previously reported dual band LNAs with these findings. A cascode arrangement was used to increase gain in [1]. [10] used the cascode common source inductive degeneration architecture to accomplish power restricted simultaneous noise and input matching at 2.4 and 5.2 GHz. [18] used the LC parallel resonance and LC series networks to accomplish dual band input impedance matching and noise matching using a small-size capacitor and linked inductor for gain improvement. [19] used the current-reuse approach to decrease power dissipation. Finally, in [20], a linearization approach was applied to improve the input third-order intercept point (IIP3), and an enhanced output matching network was built for wireless and

Bluetooth applications utilising 65 nm CMOS technology. This suggested dual band LNA has a lower power consumption of 2.39 mW with a low supply voltage while keeping comparable other metrics.

Table 1
Comparison of performance with previously published dual band LNA

Parameter	[1]*	[10]	[19]*	[21]	[22]	This work
CMOS Technology(µm)	0.13	0.13	0.13	0.18	0.65	0.13
Frequency (GHz)	2.4	2.4	2.4	2.4	2.4	2.4
	5.2	5.2	5.2	5.2	5.2	5.2
Supply Voltage (V)	1.2	1.2	1.2	1.5	1.0	0.5
S21 (dB)	21.8	19.3	17.1	15.1	14.24	15.8
	14.2	17.5	8.5	13	11	11.7
S11 (dB)	-18	-16.8	-15.6	-13.3	-24.3	-12.3
	-16	-19.4	-13.8	-12.4	-26.4	-14.2
S22 (dB)	-14	-23.5	N/A	N/A	N/A	-14.4
	-16	-27.8	N/A	N/A	N/A	-11.2
IIP3 (dBm)	7	-20.1	N/A	-16	-1.66	-12.4
	10	-18.1	N/A	-10	0.04	-20
NF (dB)	4.1	3.2	3.6	2.7	2.4	2.97
	5.0	3.3	3.3	3.2	4.5	4.23
Power (mW)	32.9	2.4	9.8	2.49	3.6	2.39

*post-layout simulation

4. Conclusions

This study emphasises the use of the forward body bias approach to reduce threshold voltage, resulting in a considerable reduction in power usage. A notch filter approach is also used to produce good input-output matching at 2.4 and 5.2 GHz. According to pre-layout simulation findings, the suggested dual-band LNA consumes 2.39 mW from a 0.5 V power source. Overall, the results show that the parameters are acceptable and that WLAN applications have promise.

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