SEMARAK ILMU PUBLISHING

Journal of Advanced Research in Applied Sciences and Engineering Technology

Journal homepage:
https://semarakilmu.com.my/journals/index.php/applied_sciences_eng_tech/index
ISSN: 2462-1943

Design of Class E CMOS Power Amplifier with Integrated Active Inductor for 5G Applications

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ARTICLE INFO

Article history:
Received
Received in revised form
Accepted
Available online

Keywords:
Class E; power amplifier; active inductor; CMOS; passive inductor; power added efficiency

ABSTRACT

This paper presents a design of class E power amplifier (PA) with integrated active inductor for 5G applications. A high Q-factor active inductor (AI) is proposed utilizing CMOS 0.18-µm technology. A Gyrator-C based is employed to realize an active inductor with a double cascode resistive feedback configuration. The biasing voltage of 1.21 V, current source of 0.5 mA and supply voltage of 2.5 V is used. In order to obtain high efficiency, the proposed AI is implemented in a class E power amplifier by replacing on of the spiral inductors. According to the simulation results, the proposed AI can reach a high Q-factor of 50,000 and an inductance of 2.03 nH at 3.5 GHz. The power added efficiency (PAE) of CMOS class E PA with integrated AI, according to simulation result, is 72 % at 3.5 GHz. The intended PA's PAE was dramatically raised by the class E AI that was built.

1. Introduction

Spiral inductors are frequently employed in radio frequency (RF) front end designs, such as low noise amplifiers, power amplifiers, mixers, and others, to achieve input and output impedance matching [1]. The large, heavy passive inductors used in RF designs are typically maintained off the chip. However, on-chip spiral inductors take up a lot of room in the die area [2]. In order to replace the spiral inductor, an active inductor (AI) is suggested [3-6].

The active inductors are used to replace on-chip spiral inductors mainly due to high quality factor. Due to the small silicon area, the active inductors are highly adjustable and the cost of manufacture
can be decreased. It has numerous types and construction methods to produce active inductors for varied applications [7].

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https://doi.org/10.37934/araset.63.2.5666

The active inductors are used to replace on-chip spiral inductors mainly due to high quality factor. Due to the small silicon area, the active inductors are highly adjustable and the cost of manufacture can be decreased. It has numerous types and construction methods to produce active inductors for varied applications [8].

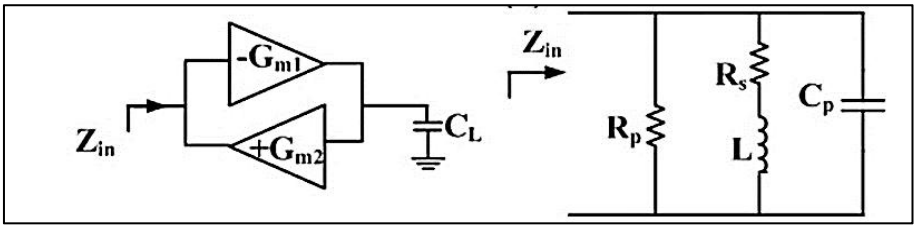
When it comes to layout, passive inductors take up more space, but active inductors are more tolerant of available space [9]. Due to its limited silicon area and excellent tunability, it is less expensive to manufacture. Low Q factors in passive inductors result in significant energy rate losses, which hastens the decay of oscillations. Due to the fixed circuit tunability of the passive inductor, which requires a wide bandwidth to amplify the signal, more energy is lost. The performance of a chip will be impacted as a result of the major EMI problem that the passive inductor experienced because it introduces unwanted noise or interference to the circuit, delaying the transfer of signals and resulting in poor connectivity between electrical. The tuning range and Q factor of an active inductor are both high, and it is EMI-resistant. Therefore, active inductors are chosen over passive inductors in IC design. To increase AI performance and cut costs, some problems with current AI have been identified, including the need to build high Q-factor AI with small transistor size, high resonant frequency, and low power consumption.

The most recent generation of wireless networks, or 5G, can provide extremely high data speeds, low latency, excellent dependability, and large amounts of capacity for devices today [10-11]. The performance of 5G, however, is heavily reliant on our current closeness to the cell site. Three layers make up the 5G spectrum band: low, mid, and high band. Low band frequencies are below 1 GHz, mid band frequencies are between 1 GHz and 6 GHz, and high band frequencies are between 24 GHz and 40 GHz. Broad coverage is offered by low band spectrum or 5G networks, however speed and latency are only marginally superior to those of 4G networks. It is perfect for 5G since it can carry a lot of data and travel a long distance, and the mid band spectrum of 5G can provide both coverage and capacity. According to the GSMA, the optimal 5G band range, which may be used in most countries, is between 3.3 GHz and 3.8 GHz [12-14]. Since high band 5G spectrum operates at a higher frequency than low and mid band spectrum, it can transport data at a very fast rate but has a limited range. For mobile services, the GSMA suggests using the 26 GHz, 40 GHz, 50 GHz, and 66 GHz bands. However, the association also points out that there is already significant momentum for spectrum in the 26 GHz and 28 GHz channels because they are close together and hence easier for devices to handle [15].

In this paper, a Gyrator-C based high Q-factor AI is proposed and implemented using a double cascode resistive feedback architecture. High-Q factor is achievable by properly biasing the voltage and current source. To boost efficiency, the proposed AI is further integrated with class-E PA. The CMOS 0.18-m technology is used to implement the proposed PA with AI.

2. Gyrator-C Active Inductor

Gyrator-C based active inductors are frequently utilized because they require small chip area and exhibit improved linearity, especially at sub-GHz. Capacitance must be applied to the output port of the Gyrator in order to produce the Gyrator-C AI from the ideal Gyrator-C [16]. The actual Gyrator-C based AI block design is shown in Figure 1, and its corresponding circuit is shown in Figure 1(b) [17].



(a) (b)

Fig. 1. (a) Gyrator-C based AI block diagram (b) Gyrator-C based AI equivalent circuit [15]

The equivalent inductance and impedance are shown in Eqs. (1) and (2). Since the complex frequency, s, is identical to jω, Eqs. (1) and (2) may be compared to show that the input impedance Z_{in} is exactly proportional to frequency. Eq. (3) demonstrates the inductive nature of the impedance at the output port. Consequently, active inductor is created using the gyrator-C network. Gyrator-C active inductor is the name given to this synthesized inductor. The product of the transconductances of the transconductors and the load capacitance, C determine the inductance of an active inductor, which is inversely proportional to the product. In a real active inductor circuit, parallel capacitance C_p, series resistance R_s, and parallel resistance R_p may also be present in addition to the inductance.

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{sC}{G_{m1}G_{m2}} \quad (1)$$

$$Z_{in} = \frac{V_{in}}{I_{in}} = sL \quad (2)$$

$$L = \frac{C}{G_{m1}G_{m2}} \quad (3)$$

For CMOS active inductor, once the input impedance is derived, then quality factor Q can be defined as shown in the Eq. (4), which Im (*Zin*) is the imaginary part of the inductor input impedance and Re (*Zin*) is the real part of the inductor input impedance.

After determining the input impedance for a CMOS active inductor, the quality factor Q may be determined as indicated in Eq. (4), where Im_{Zin} denotes the imaginary portion of the inductor input impedance and Re_{Zin} denotes the real portion.

$$Q = \frac{\mathrm{Im}_{Zin}}{\mathrm{Re}_{Zin}} \quad (4)$$

3. Proposed Design of Active Inductor

The proposed AI using cascoding method to improve output impedance, gain and Q-factor as it can reduce the series resistance, Rs loss. Figure 2 shows the equivalent circuit for RL series to parallel transformation. The cascading method can also adjust the parallel resistance, Rp loss which

generated from Rs after transformation from series to parallel of equivalent circuit due to Gyrator theory. The equivalent circuit for RL series to parallel transformation was shown in Figure 3.

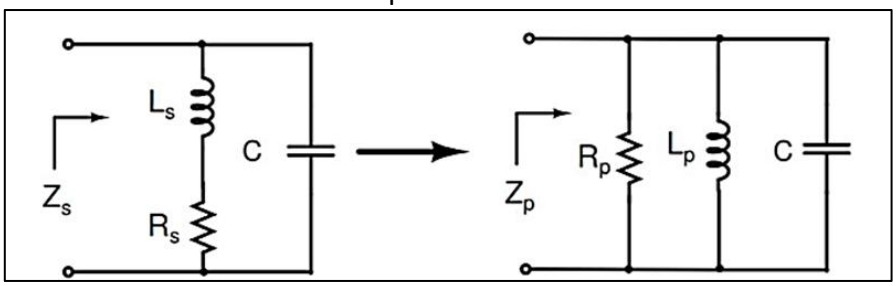


Fig. 2. The equivalent circuit for RL series to parallel transformation

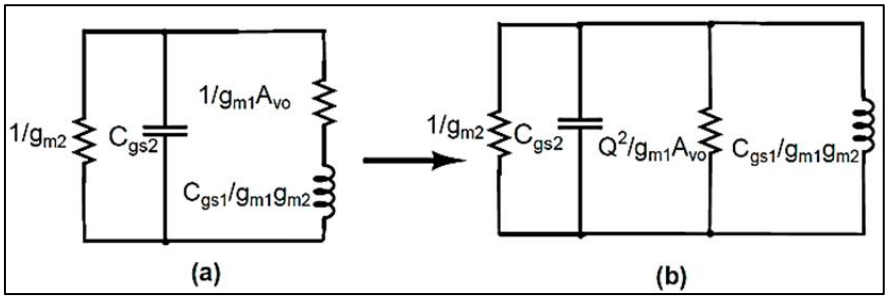


Fig. 3. (a) RL equivalent circuit (b) RL narrow band approximation

Figure 4 shows the proposed CMOS active inductor using CMOS 0.18-µm technology. The suggested CMOS active inductor employing CMOS 0.18-m technology is depicted in Figure 4. Q-factor was unable to increase further due to the coupling path from Cgs1 and Cgs2, which is depicted in Figure 3(b). To increase Q-factor and balance the surplus current in the capacitances, a long tail pair transconductor and positive feedback surrounding input transistor, M2, were required. M2 and M3 were cascoded by M7 and M8, respectively, to adjust the Q-factor. M4 through M6 were added as current sources. The AI total parallel resistive loss is adjusted using the biasing voltage VB. The frequency of the AI self-resonant system was controlled by the current I1.

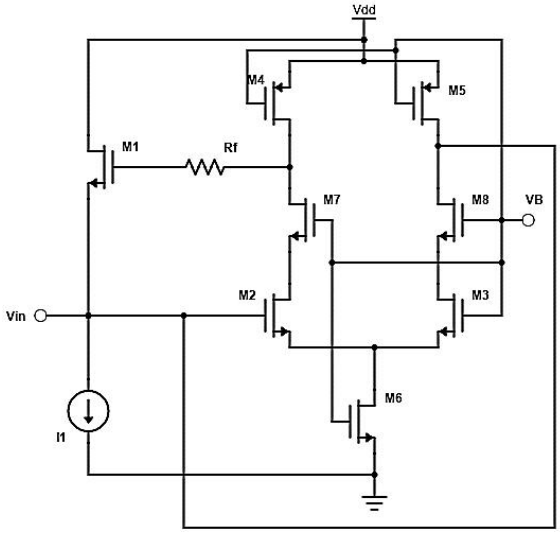


Fig. 4. Proposed CMOS AI Circuit

According to Figure 4, the capacitor between M1 and M2 is charged by Vin, which is converted into current by M2, M3, current from M4 and M5, and current in M6. The capacitor's voltage is then converted back to input current by M1. Positive feedback, however, occurs when current from

M4 rises and current from M5 falls as a result of rising Vin, as current in M6 is the constant sum of current from M4 and M5. As a result, Vin increases more and M3 drain voltage rises. The equation for quality factor of the double cascode AI is shown in Eq. (5) below.

$$Q = \sqrt{g_{m1} g_{m2} C_{gs1} C_{gs2}} \left[\frac{1}{\frac{C_{gs2}}{r_{ds2}} + \frac{2C_{gs1}}{r_{ds1}}} \right] \tag{5}$$

Table 1 lists each component, supply voltage, and biasing. The transistor gate length used in this CMOS AI architecture is 0.18-µm. To achieve high Q-factor AI, the current source is set at 0.5 mA, the biasing voltage and Rf are optimized and set at 1.21 V and 390 Ω, respectively.

Table 1
AI components and its parameters the table

Components	Parameters
M1	9 µm/0.18 µm (NF=5)
M2 = M3	1 µm/0.18 µm (NF=24)
M4 = M5	1 µm/0.18 µm (NF=2)
M7 = M8	10 µm/0.18 µm (NF=2)
M6	5 µm/0.18 µm (NF=5)
Rf	390 Ω
Vdd	2.5 V
VB	1.21 V
I1	0.5 mA

4. Class E PA with Active Inductor

Figure 5 shows the class E PA circuit with the proposed AI. The inductors L1, L2, L3 and L4 with value of 8.42 nH, 6.99 nH, 3.33 nH and 1.47nH, respectively. A spiral inductor of 1.47 nH in the previously published PA is replaced with the proposed AI [11]. The drain of Q3 in PA is connected with drain of M4 and M7 around Rf while the other node is connected with Vin or I1 of the AI after L4 is being taken out. The class E PA in Figure 5 is simulated using Cadence virtuoso for the performance analysis.

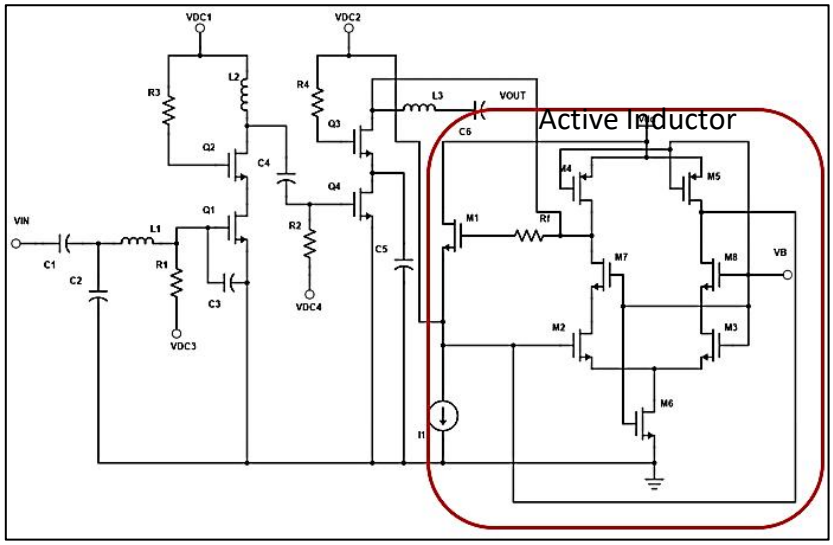


Fig. 5. Proposed CMOS class E PA with AI

5. Results

5.1 Active Inductor

The proposed AI is simulated using Cadence Virtuoso Analog Design Environment. The supply voltage Vdd of 2.5 V, biasing voltage VB of 1.21 V and current source I1 of 0.5 mA is used during simulation. The proposed AI's real and imaginary impedance with 1.21 V of biasing voltage is shown in Figure 6. At 3.5 GHz, the imaginary value is 46.85 Ω, but the real value is almost 0 Ω. The proposed AI's real and imaginary impedance with 1.21 V of biasing voltage is shown in Figure 6. At 3.5 GHz, the imaginary value is 46.85, but the real value is almost zero ohm. From frequencies of 0.5 GHz to 6.5 GHz, the imaginary impedance is higher than the real impedance, indicating that energy storage provided by inductance is predominating over energy losses owing to resistance. As a result, a high Q-factor is attained. The proposed AI's Q-factor with a 1.21 V biasing voltage is shown in Figure 7. The simulation results demonstrated that the Q-factor of 50K is seen at 3.5 GHz, as can be seen.

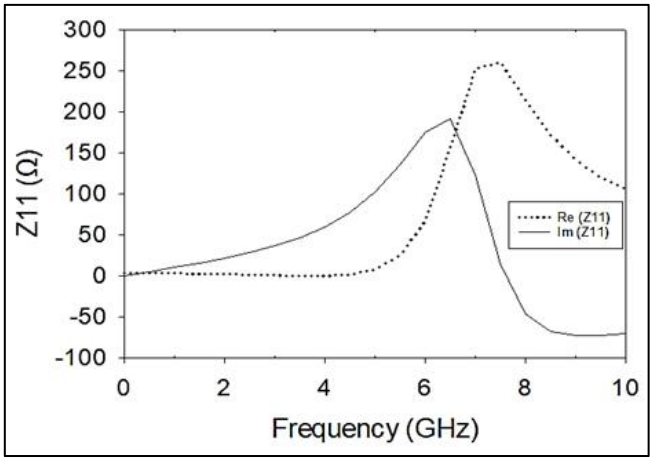


Fig. 6. Real and imaginary impedance of the proposed AI

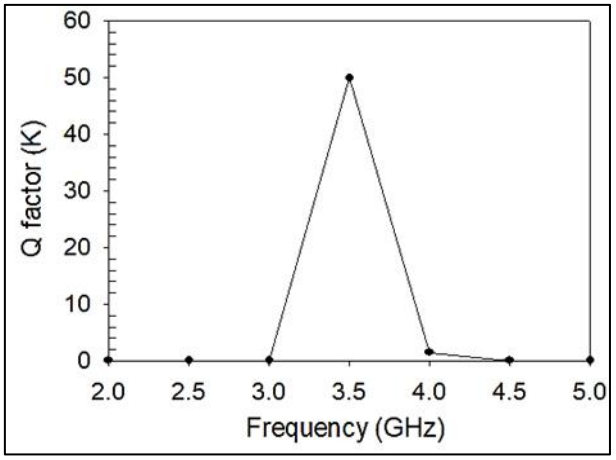


Fig. 7. Q-factor of proposed AI with 1.21 V VB

When the current source I1 is changed from 500 A to 505 A, the Q-factor is shown in Figure 8. As can be seen, the Q-factor at 3.5 GHz reduced from 50k to 7.30k by raising the biasing current by around 1 A. The inductance vs frequency of an AI with a 50k Q-factor is shown in Figure 9. At

frequencies ranging from 1 GHz to 7 GHz, the inductance of AI varies from 2.05 nH to 4.92 nH. As can be seen, at 6.5 GHz, the higher inductance values were 4.92 nH.

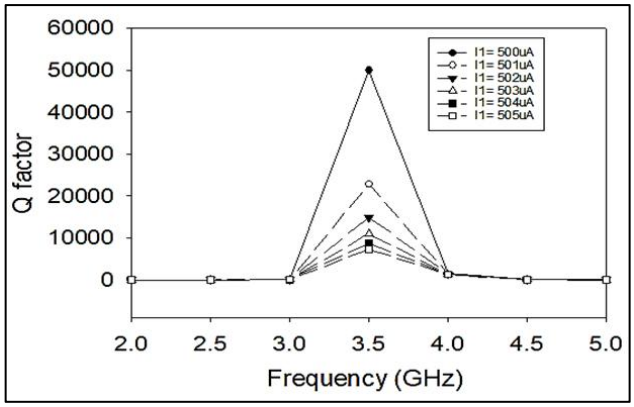


Fig. 8. Q-factor when vary current of current source I1

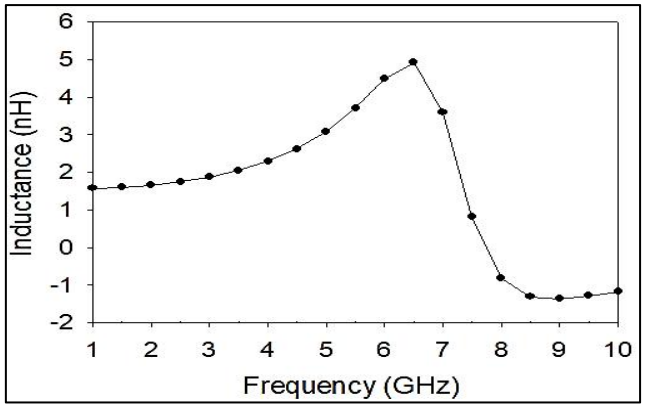


Fig. 9. Inductance of AI with 50K Q-factor

5.2 Class E PA with AI

The power added efficiency (PAE) of the simulated PA with the suggested AI is shown in Figure 10. As can be observed, the 50k Q-factor AI results in a high PAE of 72% at input power of -5 dBm. However, the PAE is decreased to 51.15% at input power of -5 dBm when the Q-factor of 6.12k AI was applied in the PA. Similar to this, when the Q-factor of AI is 455, the PAE of PA is decreased to 40.32%. The s-parameter of PA with suggested AI is shown in Figure 11. With a gain of 19.52 dB, the input return loss, S11, of -29.24 dB and the output return loss, S22, of -30.34 dB are attained.

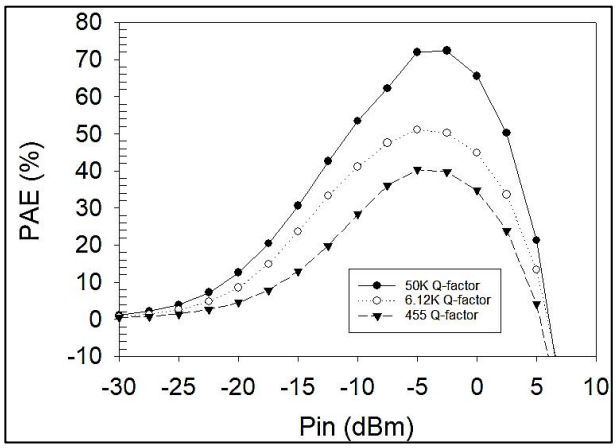


Fig. 10. PAE of PA with 50K, 6.12K and 455 Q-factor AI

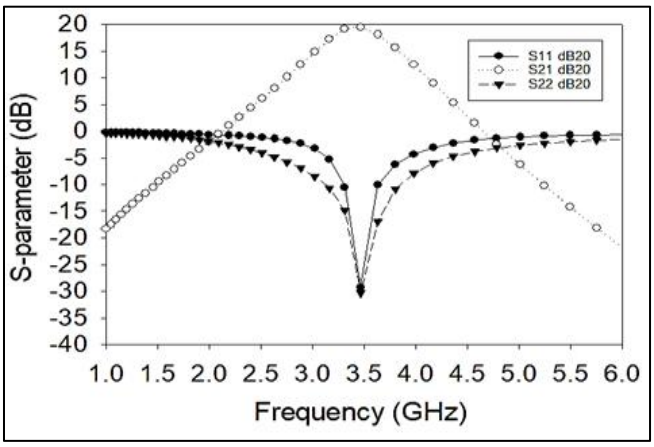


Fig. 11. S-Parameter of PA with proposed 50K Q-factor AI

Figure 12 displays the stability factor of the suggested PA with AI. Since Kf value is bigger than 1, the suggested PA with AI is unconditionally stable from 1 GHz to 6.5 GHz. The power amplifier's feedback network is built to provide enough stability margins and guard against unwanted oscillation or instability.

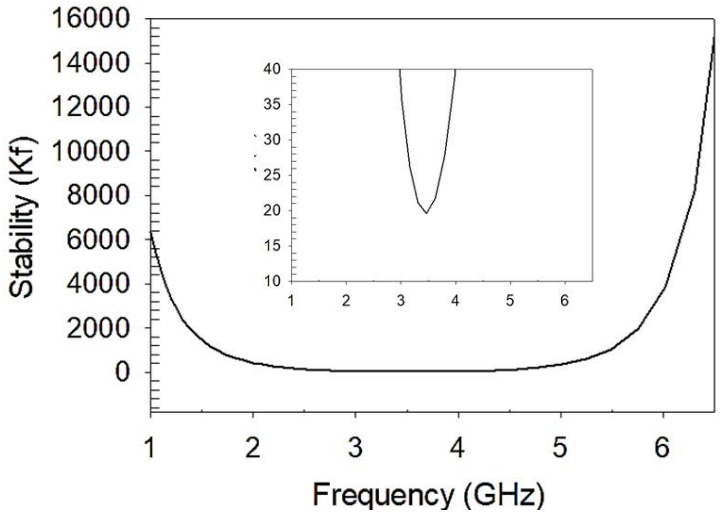


Fig. 12. Stability of PA with proposed 50K Q-factor AI

Meanwhile, Figure 13 showed the linearity of the proposed PA with AI. It is simulated in Cadence utilizing PAC in periodic steady-state PSS. It was noted that the P1dB and IIP3 were, respectively, -15 dBm and -3 dBm. The IIP3 interception happened at 3.5 GHz with an output level of 20 dBm.

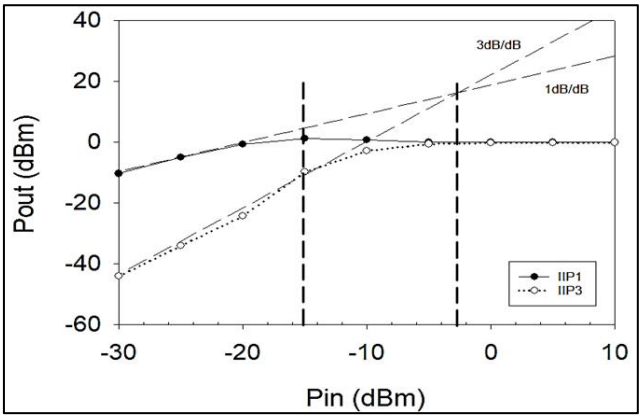
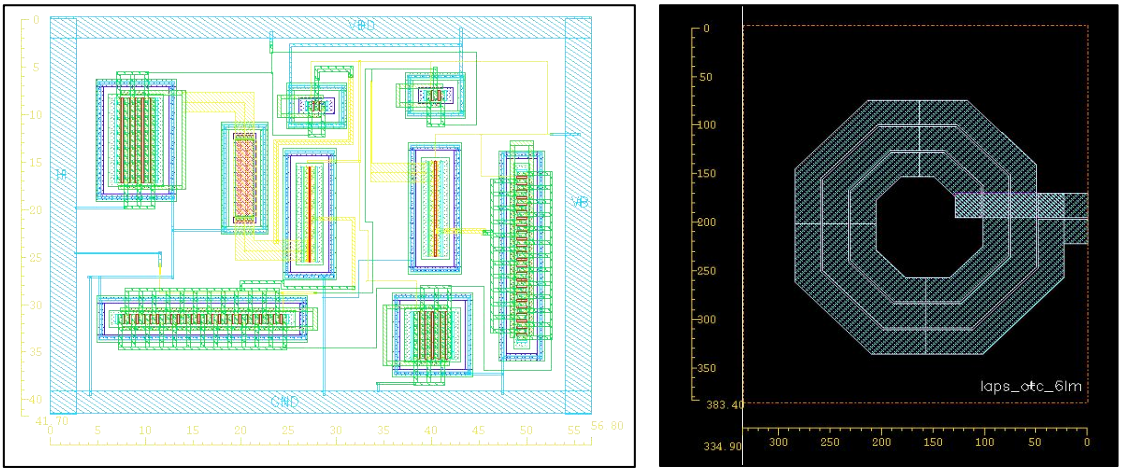


Fig. 13. Linearity of PA with proposed 50K Q-factor AI

Figure 14 shows the layout of the proposed AI and on chip spiral inductor at 2.03 nH. AI has a total area of 2.37 mm^2. The spiral inductor layout measures 128.4 mm^2 in dimension. As can be shown, AI may minimize the on-chip area by around 98 %.

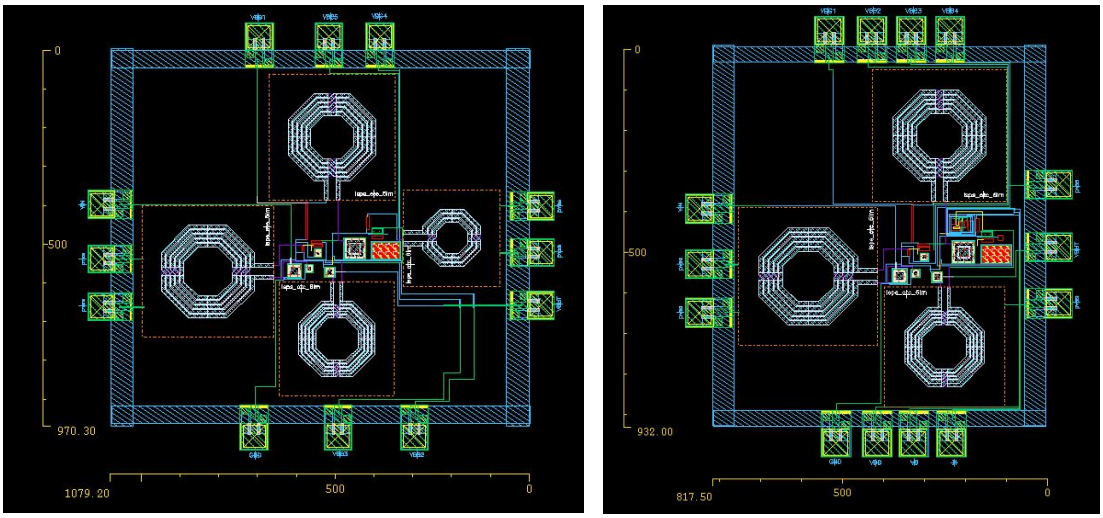


(a) (b)

Fig. 14. (a) Layout design of the proposed AI (b) Layout of spiral inductor

The design of the original PA and the suggested PA with AI are depicted in Figure 15. A 1.04 mm^2 is the overall size of the original PA, while 0.76 mm^2 is the total area of the PA with AI. As can be observed, using AI, the overall PA area may be decreased by roughly 73 %.

The performance of the active inductors in comparison to previously published works is shown in Table 2. The proposed AI, as can be observed, achieved a higher Q-factor of 50k at 3.5 GHz. Table 3 displays the performance of the original PA and the AI-added PA. A class E PA with AI reaches a high Q-factor and higher power added efficiency.



(a) (b)

Fig. 15. (a) Original layout class E PA (b) Layout PA with AI

Table 2
AI performance comparison with previous works

Ref	[18]	[19]	[20]	[21]	This work
CMOS tech (µm)	0.18	0.35	0.13	0.18	0.18
Vdd (V)	1.8	1.4	1.0	1.8	2.5
Frequency range (GHz)	2.4	0.5-1.0	2-2.6	0.9-2.75	3.5
Inductance tuning (nH)	10.8	350	1.5-17	5.46	2.03
Max Q-factor	6.36	>120	320	21000	50000
Pdc (mW)	0.453	0.4	0.9-1.3	3.37	37.7

Table 3
Original class E PA and PA with AI performance comparison

Class E PA	Original PA	PA with AI		
		50k Q-factor	6.12k Q-factor	455 Q-factor
PAE (%)	50	72	51.15	40.32
S21 (dB)	19	19.52	18.24	16.11
Power Gain (dB)	22.5	20	N/A	N/A
Size (mm^2)	1.047	0.762	N/A	N/A

6. Conclusions

Design and simulation of the active inductor with a high Q-factor are successful. To attain a high Q-factor, a Gyrator-C based AI with a double cascode resistive feedback setup is proposed. In order to improve efficiency, the proposed AI is additionally combined with a class E PA by replacing the spiral inductor. According to the simulation results, the proposed AI at 3.5 GHz and a 2.03 nH inductance achieved a high Q-factor of 50k. Additionally, the class-E PA with AI shows a 72 % increase in power added efficiency (PAE). In addition, compared to a spiral inductor, the overall area of AI can be reduced by around 98 %. When AI is used, the area of class E PA is decreased to 73 %. The PAE of the proposed PA and the total on chip area are both greatly increased and decreased by the incorporation of AI in class E PA.

Acknowledgement
The author would like to acknowledge the support from the Fundamental Research Grant Scheme (FRGS) under a grant number of FRGS/1/2020/TK0/UNIMAP/02/26 from the Ministry of Higher Education Malaysia.

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