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A Fully Differential Active Inductor with Cascode Current Mirror Using 0.18-um Technology for RF Frequency

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ABSTRACT

This paper introduces a fully differential CMOS active inductor (AI) integrated with a cascoded current mirror, tailored for applications within the RF frequency range. The active inductor design is meticulously realized using CMOS 0.18-µm technology. The circuit implementation comprises a fully differential cross-coupled pair of transistors, strategically employed to impart negative feedback, thereby enhancing the quality factor (Q). The cascoded current mirror functions as a pivotal biasing component, facilitating control over the current source to modulate negative feedback and Q factor tuning. Simultaneously, two resistors integrated into the differential structure are crucial in managing the frequency spectrum. Simulation results substantiate a Q factor of 16k, coupled with an inductance of 14 nH, prominently achieved at 3 GHz frequency. Additionally, the objective of achieving a robust Q factor at 3.5 GHz, amounting to 500, is successfully realized. Noteworthy is the adaptability in achieving a frequency range spanning 2 GHz to 3.6 GHz by manipulating resistor values. Furthermore, the study observes that manipulation of supply voltage and current source enables the tuning of Q factor values from 70 to 16k. A performance assessment, juxtaposed with previously published works, underscores the viability of the proposed active inductor for applications within the gigahertz frequency range of RF.

1. Introduction

Inductors hold significance within circuits as they primarily function to impede high-frequency signals and counteract abrupt current changes resulting from signal fluctuations. This fundamental role involves both blocking high-frequency components and resisting rapid current variations in their basic configuration [1]. The conventional inductor, commonly referred to as a passive or spiral inductor, is recognized for its coiled wire configuration. Historically positioned as off-chip components, these inductors exhibit advantageous traits such as linearity and minimal phase noise when integrated within circuits [2-3].

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Nevertheless, they are not exempt from limitations. Their notable drawbacks encompass significant silicon space consumption due to their multi-turn nature. The substantial dimensions of the inductor contribute to the overall enlargement of the chip, thereby elevating both the size and cost of the integrated circuit [4] alongside challenges in achieving high-quality factors [5], fixed and restricted inductance levels, and constrained self-resonant frequencies [2].

To combat these shortcomings, the development of AI has been proposed, which can have a higher Q factor and smaller chip size [6] and its impedance can be varied with frequency [7, 8]. This can be beneficial in many applications that require it, like power amplifiers which was the purpose in [9] to make a PA with no spiral inductor. Especially since the different classes of PA do not have the highest efficiencies in their practical use and 100% efficiency is in ideal situations [10].

Still, the AI is not perfect, the higher Q factor and smaller size come at a cost. It consumes high power since it is an active component and it is necessary to reach high Q factor values, while also having worse linearity compared to the spiral inductor [11-13]. These limitations may dictate the usage of AI, and because of that, there are 2 main methods to design AI either as an op-amp or gyrator-C [14]. The op-amp is suitable for the lower frequency spectrum, up to the MHz range. But, the gyrator-c, is based on the concept of the gyrator. This idea was subsequently refined into the Gyrator-C configuration, which later served as the foundation for the development of AI.

Relating to a previous study in [15], that was focusing on the pre-layout simulation. Which achieved a Q factor of 12.5 K. This paper focuses on the post-layout and proposes a fully differential AI integrated with a cascoded current mirror to enhance its Q factor. The AI design is implemented using CMOS 0.18-µm technology. The AI circuit design is explained in Section II, simulation results are presented in Section III, and concluding remarks are provided in Section IV.

2. Methodology

2.1 Circuit Design

The circuit proposed in this work presents a comprehensive design for a high-performance AI with the primary objective of enhancing the Q factor through the integration of differential operation and negative feedback.

Figure 1 shows the circuit design and its testing using Cadence Virtuoso, the active inductor circuit's performance is evaluated through extensive simulations, considering various operating conditions and performance metrics, including the Q factor, power efficiency, and frequency response. Detailed analysis of the cascode current mirror's component values, transistor sizes, and biasing conditions is conducted to understand its impact on the circuit's behavior.

The core components of the active inductor circuit include six transistors: M1, M2, M3, M4, M5, and M6. Transistors M3, M4, M5, and M6 are directly connected to the VDD to establish suitable biasing conditions. However, transistors M1 and M2 are controlled by reverse biasing, regulated through resistors connected to the gate terminals of M5 and M6. This dynamic control mechanism allows for precise manipulation of M1 and M2. The gate of the NMOS devices is biased in the same way, while also connected to the drain of the PMOS transistors.

A cascode current mirror configuration is utilized to provide stable and accurate biasing currents to transistors M1, M2, M3, and M4. It consists of M7, M8, M9 and M10. The cascode current mirror ensures a high level of impedance observed by the active inductor, enabling increased control over the Q factor. Furthermore, it minimizes the influence of the transistor's Early effect, contributing to improved linearity and stability. The cascoded current mirror is utilized as a biasing mechanism to regulate the current source, enabling the manipulation of negative feedback, and facilitating the tuning of the Q factor. By mitigating energy losses, the negative

feedback loop enhances energy storage efficiency, resulting in a higher Q factor. The active inductor circuit is optimized for stability and performance through the negative feedback configuration.

Figure 2 presents a more comprehensive representation of this design, showcasing the inclusion of both the current mirror biasing voltage and resistor. However, the chip area can be further optimized to reduce the size. Both elements are interlinked, serving as the source for the current mirror. Notably, Metal 1 interconnects with both VDD and GND within this circuit configuration. Meanwhile, VIN, along with the IN and OUT ports, is linked via Metal 2. The remaining circuitry interfaces with Metal 2 and Metal 3 in accordance with each designated port. The distances maintained between individual terminals play a pivotal role in preserving the high Q factor; diminishing these distances could further compromise the Q factor. Consequently, meticulous optimization ensures that these distances remain conducive to sustaining the high Q factor, as opposed to clustering components in proximity.

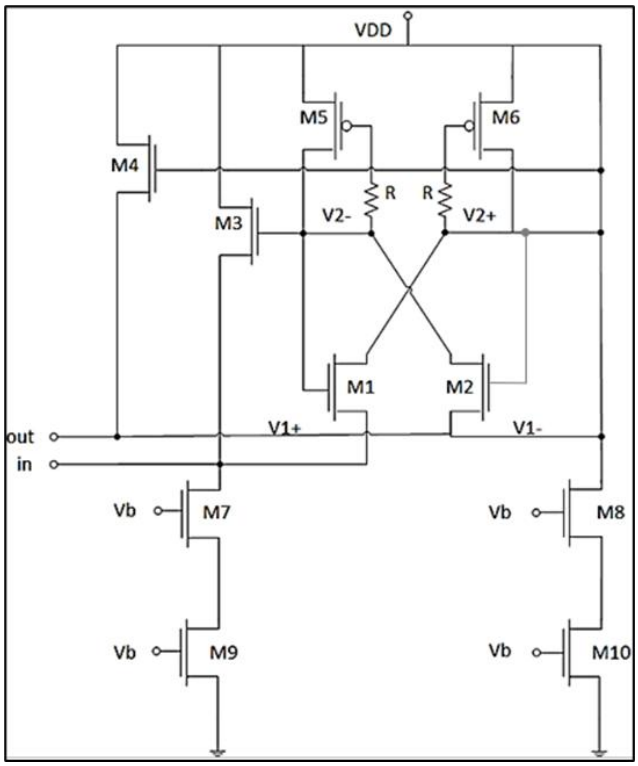

Fig. 1. Circuit design of the proposed Active Inductor (full circuit for current mirror is excluded)

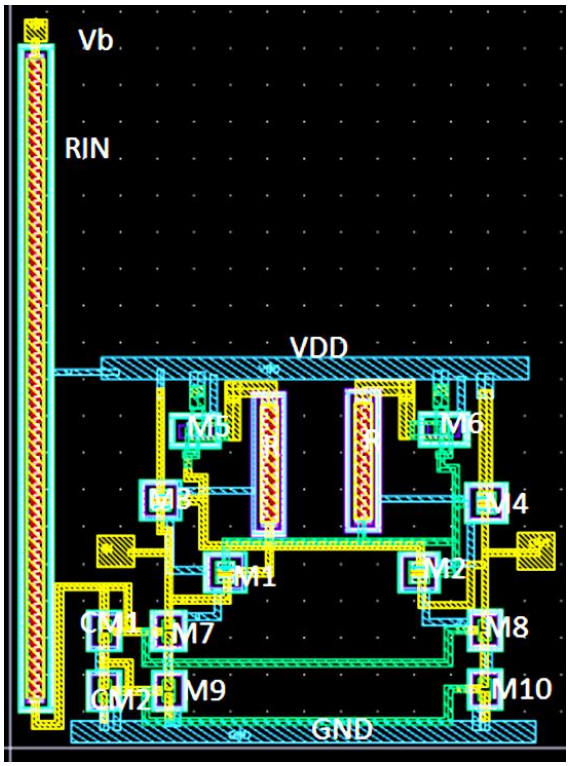

Fig. 2. Layout design of the proposed Active Inductor

3. Results

3.1 Pressure Distribution

The circuit design uses Silterra's 0.18-µm technology, and as stated previously it is tested through Cadence Virtuoso software, in both schematic and layout. The following results will focus on the post-layout simulation.

The dimensions of the transistors are seen in Table 1, it shows each group of them separately. Since both M1 and M2 are the transistors that are fed from the differential loop. M3 and M4 are the NMOS transistors that are connected directly to the VDD, and both M5 and M6 are PMOS that feed the whole circuit. Transistors from M7-M12 are the cascode current mirror that controls the current biasing of the circuit.

Table 1
Transistor dimensions

Transistor	Dimensions ((No. of finger X W)/ L)
M1, M2	(3 x 1 µm) / 0.18 µm
M3, M4	(2 x 1 µm) / 0.18 µm
M5, M6	(2 x 1 µm) / 0.18 µm
M7, M8, M9, M10	(1 x 1 µm) / 0.18 µm

Since the 3.5 GHz frequency band is the focus of this study, Figure 3 shows the frequency response of the AI under consideration, with an emphasis on the RF frequency range. The impedance behavior of the AI at various frequencies is clearly visible in the frequency response graph.The imaginary portion of the AI's impedance has a peak value of around 310 in the RF region, indicating the AI's reactive nature at frequencies in this band. Additionally, the peak value of the real part of the AI is 0.63 at 3.5 GHz in the same region but reaches up to 350, which points to a dominant resistive behavior at specific frequencies after 3.6 GHz.

Moreover, the frequency range where the AI operates efficiently is predominantly centered around the range of 3-3.5 GHz, suggesting a resonance or optimum performance point nearby. Beyond this amount, the AI's performance deteriorates noticeably and presents greatly reduced impedance values, which could negatively impact the functionality of the AI.

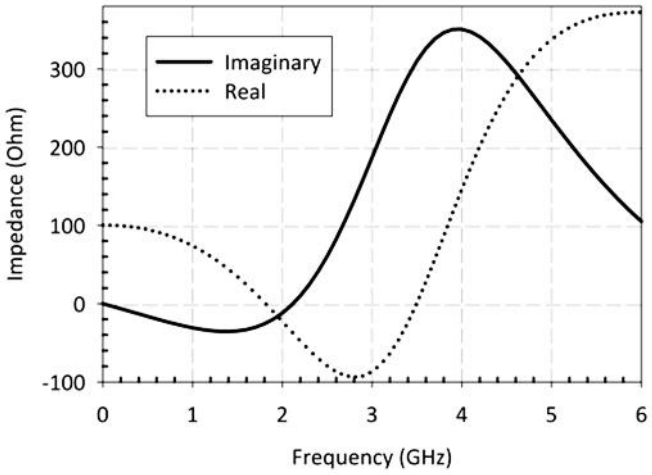

Fig. 3. Impedance matching from the active inductor at 3-3.5 GHz frequency range

As is shown in Figure 4, the best value for improving the Q factor at the desired frequency of 3.5 GHz has been found to be setting the biasing voltage at 0.93 V. To obtain the appropriate Q factor performance precisely at the set frequency, the resistance is fixed at 14 kΩ. By changing the biasing of the current mirror, more precisely by varying either the Vb or the resistor linked to it, the Q factor of the AI can be actively controlled. However, it is shown that when compared to the biasing voltage, changing the resistance has a comparatively modest effect on the Q factor.

By modifying the transistor's size and feedback resistance, the frequency of the active inductor can be adjusted. Higher frequencies, however, lead to lower Q factors. Figure 5 depicts the frequency response at 3.0 GHz, 3.3 GHz, and 3.6 GHz, with 3.6 GHz being the highest frequency where the chosen parameters will still produce an acceptable Q factor. The active inductor displayed a Q factor of 500 at 3.5 GHz, successfully attaining the main objective of a high Q factor at this frequency, while it declines at higher frequencies. The key to the design's effectiveness is

adjusting the feedback resistance and transistor size for effective resonance and selectivity at 3.5 GHz.

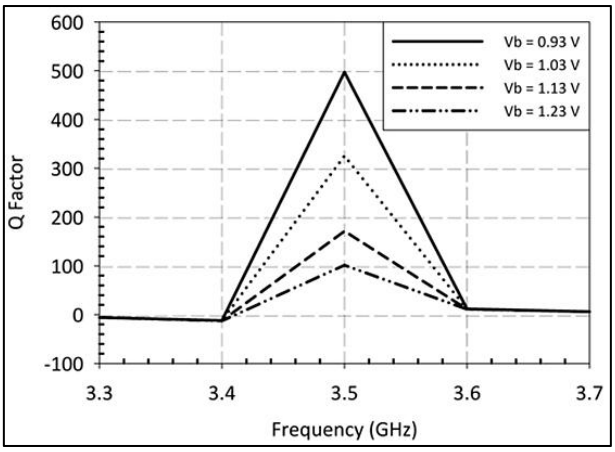

Fig. 4. Q factor control using Vb

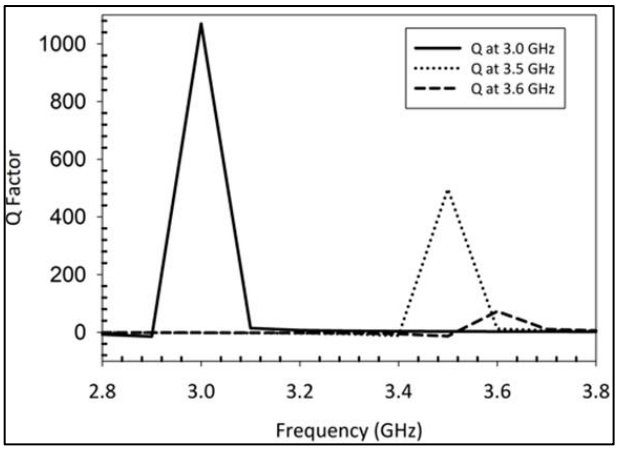

Fig. 5. Q factor at a different range of frequencies from 3-3.6 GHz

Figure 6 points to the highest Q factor that this design can show at 16K, which is achievable at 3 GHz with a Vb of 0.93. However, the graph shows that it is not a smooth change to reach. Meaning, the line in which the Q factor is shown is a bit curved around the edges and does not show a straight line for the change in Q, compared to other Q factor measurements as shown in Figure 5.

The AI's inductance is significantly impacted by changing the VDD value. The inductance level of the AI rises as the VDD voltage is reduced. Figure 6. illustrates this link between VDD and inductance, with all values determined particularly for the frequency of 3.5 GHz, which is exactly at 14.1 nH and can be achieved at 2.3 V. The observed pattern in Figure 7 demonstrates the exact relationship between the inductance of the AI and the VDD voltage level. The inductor's value is effectively increased by reducing the VDD voltage, which has significant effects on the circuit's general functionality and behavior. The highest L can reach up to 19 nH.

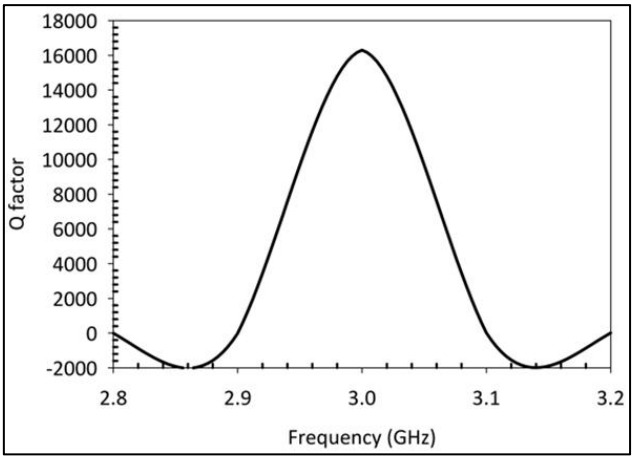

Fig. 6. The highest Q factor possible at more than 3 GHz frequency

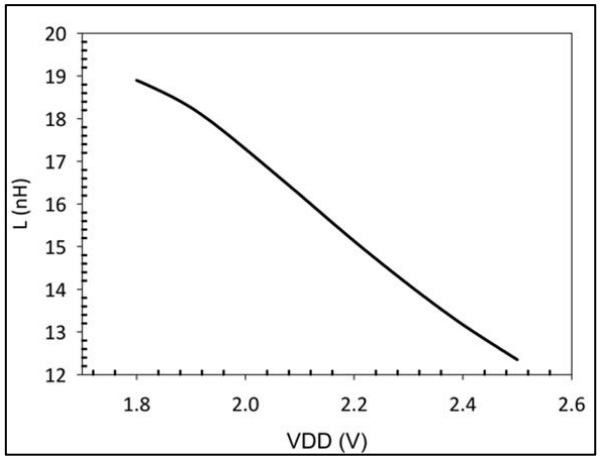

Fig. 7. Impact of VDD on the inductance values of the AI

Table 2 below shows a comparison between previous studies and the proposed circuit. It demonstrates that it can reach a higher Q factor in the post-layout simulation and with both high enough frequency and inductance range compared to the rest. However, it still consumes much higher power, and the frequency range is at 1.6 GHz bandwidth.

Table 2
Performance summary of the proposed AI compared to previous works

Reference	Technology (nm)	Supply voltage (V)	Q_{MAX} factor	L (nH)	Power consumption (mW)	Frequency range (GHz)
[12]	130	2.3	0.39k	33-98	7.28	3.31
[16]	180	1.8	2.87k	18.7	1.26	1-10
[17]	180	2.0	68k	1.1	5	-
[18]	180	1.8	21k	5.46	3.37	0.9-2.75
[19]	65	1.2	4.81k	0.21.2	2	20-30
[20]	180	1.9	1.40k	14	6	0.1-5.5
[21]	65	0.9	6.83k	6.9–16.2	23.12	21.79-29.92
[22]	180	0.97-1.9	4.06k	220.95-511.34	-	4.5-5.1
This work	180	2.3	16k	6.5-24.5	18.63	2-3.6

4. Conclusions

This study proposed a fully differential CMOS active inductor featuring a cascoded current mirror, designed using 0.18-µm technology, specifically targeting RF front-end applications. The innovation lies in achieving an exceptionally high-quality factor through the integration of a fully differential active inductor with a cascoded current mirror serving as its current source. Notably, this configuration attains a remarkable Q factor of 16k at 3 GHz, offering an inductance tuning scope spanning 14 nH to 19 nH. The versatility of Q factor modulation is realized by adjusting the resistor within the current mirror and the VDD. Additionally, the frequency ranges can be effectively manipulated by modifying the resistor value within the active inductor's differential structure. The outcomes affirm that the proposed fully differential active inductor surpasses previously published works in achieving a high Q factor, rendering it apt for RF front-end applications.

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