# Novel Compact Reconfigurable Metamaterial Diplexer-Based on RF Switches for Wireless Applications

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| ARTICLE INFO | ABSTRACT |
|---|---|
| | This paper proposes a novel reconfigurable diplexer design based on metamaterial D-CRLH transformer. The D-CRLH concept provides duality in the overall response of the diplexer achieving several bands and reducing the overall size of the diplexer, the novel reconfigurable diplexer size is $39\times15mm^2$. The system achieves reconfigurability by utilizing a PIN-diode RF switching circuit in the D-CRLH load line, allowing for seamless connection and disconnection using a biasing circuit. The novel reconfigurable diplexer offers a wide band of operation of 1GHz to 4GHz with notches to cantered at bands 1.8GHz and 2.6GHz with both notches having suppression band of 300MHz. The reconfigurable diplexer covers commercially used wireless bands, making it suitable for diverse wireless communication applications. |

## 1. Introduction

The growth for the need of reconfigurable devices to suppresses frequency bands that might cause crossover or security breaches is increasing. Due to this growth new concepts are being introduced ,such as metamaterial, to help deceives achieve high frequencies with maintaining small size. The concept of the metamaterial is to create artificial materials with negative permittivity and permeability, thus giving us new structures with a special characteristic to reduces the size and support the multi passbands [1].

There are three types of typologies used for metamaterial, Composite Right/Left Hand (CRLH) and Dual Composite Right/Left Hand (D-CRLH) first introduced Caloz [1,2] and later Inductor Loaded Composite Right/Left Hand (L-CRLH) was conducted by El-Henawy *et al.,* [3], The D-CRLH structure exhibits duality with the conventional Composite Right/Left Hand (CRLH) configuration. It comprises a series parallel LC tank and a shunt series LC tank. This duality results in distinct passbands and stopband characteristics between them [2].

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Each typology can be used in many applications such as power dividers [4-7], and phase shifters [8-10]. Also resonators conducted by [11-14], filters by [1-17] and finally diplexers introduced by [18-22].

This paper proposes a novel reconfigurable diplexer designed using a D-CRLH metamaterial transformer to achieve a low pass filter with a wide bandwidth from 1GHz to 4GHz with two notches centered 1.8GHz and 2.6GHz with suppression band of 300MHz that can be switch on and off using a PIN-diode placed between load line and unit cell achieving reconfigurability, then use this transformer to design a T-Junction Diplexer with an overall size of 39x15 mm$^2$ designed on a substrate (Roger RT5880) with $\varepsilon_r$=2.2 and thickness of 1.575mm.

## 2. Novel Reconfigurable D-CRLH Transformer
### 2.1. Half-Mode D-CRLH Transformer

Half-mode D-CRLH unit cells is proposed to aid in the design of the final reconfigurable diplexer, using metamaterial equations [1] as foundation for D-CRLH unit cell equivalent circuit then translating into microstrip structure for implementation.

Since this is half-mode D-CRLH the loaded D-CRLH equivalent can be approximated to only have $L_R$ and $C_L$, the parallel LC tank, as for $L_L$ will be removed as this is half-mode D-CRLH meaning the load will be removed, only $C_R$ will remain due to parasitic effect as seen in Figure 1(a) & (b).
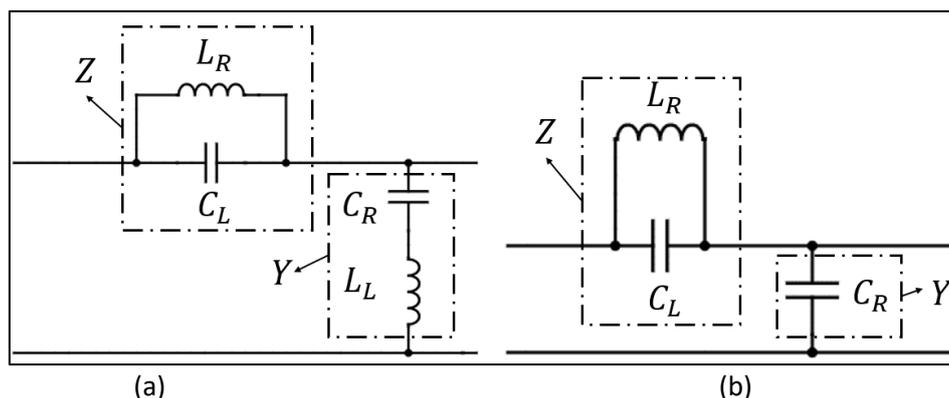


Fig. 1. Equivalent circuit for (a) Loaded D-CRLH & (b) Half-mode D-CRLH

To provide any design using half-mode D-CRLH one must obtain the cut off frequencies by satisfying the dispersion Eq. (1) at $\beta d = \pi$ and $\beta d = 0$ [1] :

$$\cos \beta d = 1 + 0.5\, Z\, Y \tag{1}$$

To obtain $Z$ and $Y$ Figure 1(b) will be referenced. Thus, resulting in,

$$Z = \frac{(j\omega L_R)\left(\frac{1}{j\omega C_L}\right)}{(j\omega L_R)+\left(\frac{1}{j\omega C_L}\right)} \tag{2}$$

$$Y = \frac{1}{(j\omega C_R)} \tag{3}$$

Then substitute Eq. (2) and Eq. (3) in Eq. (1) to obtain the following Equation.

$$\cos \beta d = 1 + 0.5 * \frac{(j\omega L_R)\left(\frac{1}{j\omega C_L}\right)}{(j\omega L_R)+\left(\frac{1}{j\omega C_L}\right)} * \frac{1}{(j\omega C_R)} \tag{4}$$

Solving Eq. (4) for be $\beta d = \pi$ will result in the cut off frequencies for two different passbands can extracted from the following Equation.

$$\frac{(j\omega L_R)\left(\frac{1}{j\omega C_L}\right)}{(j\omega L_R)+\left(\frac{1}{j\omega C_L}\right)} * \frac{1}{(j\omega C_R)} = -4 \tag{5}$$

One the other hand, the condition $\beta d = 0$ will result in upper and lower frequencies as

$$\frac{(j\omega L_R)\left(\frac{1}{j\omega C_L}\right)}{(j\omega L_R)+\left(\frac{1}{j\omega C_L}\right)} * \frac{1}{(j\omega C_R)} = 0 \tag{6}$$

Now that the equations to determine the values of $C_R$, $C_L$ and $L_R$ through the assumption of the start and end frequency, since the target is to cover most commercial band, Eq. (6) will be solved for $f = 4\text{GHz}$. Since the response will be similar to that of low pass filter.

On the other hand, the value of the insertion loss must be zero. Also, the overall characteristic impedance must be 70.7Ω. Which results in the below.

$$Z_o = \sqrt{\frac{Z}{Y}} = \sqrt{\frac{(j\omega L_R)\left(\frac{1}{j\omega C_L}\right)}{(j\omega L_R)+\left(\frac{1}{j\omega C_L}\right)} \Big/ \frac{1}{(j\omega C_R)}} = 70.7\Omega \tag{7}$$

$$S_{21} = \frac{2}{A+D+(B/Z_o)+(C*Z_o)} = \text{Zero} \tag{8}$$

For,

$$A = 1 + ZY = 1 + \frac{(j\omega L_R)\left(\frac{1}{j\omega C_L}\right)}{(j\omega L_R)+\left(\frac{1}{j\omega C_L}\right)} * \frac{1}{(j\omega C_R)}$$

$$B = Z = \frac{(j\omega L_R)\left(\frac{1}{j\omega C_L}\right)}{(j\omega L_R)+\left(\frac{1}{j\omega C_L}\right)}$$

$$C = Y = \frac{1}{(j\omega C_R)}$$

$$D = 1$$

Using Eq. (6), Eq. (7) and Eq. (8), the values of $C_R$, $C_L$ and $L_R$ can determined by solving the three equations together thought the assumption the frequency as mentioned above.

Using the circuit in Figure 1(b) as reference. A detailed circuit for half-mode D-CRLH transformers will be proposed to give more control over the simulation, by diving the basic components, $C_R$, $C_L$ and $L_R$, into several components. As shown in Figure 2.
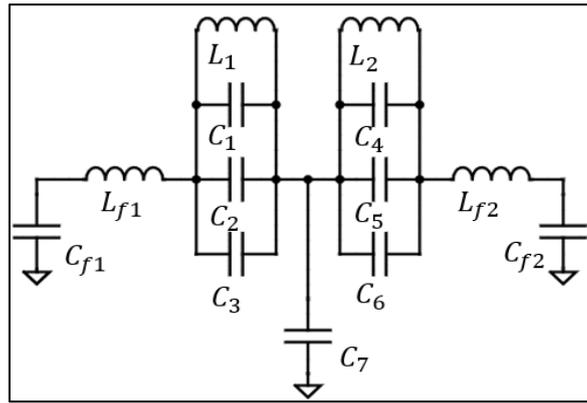
**Fig. 2.** Half-mode D-CRLH equivalent circuit

Firstly, the component $C_L$ will be calculated as 4.4005pF and divided into $C_1 = C_3 = 0.1$ pF and $C_2 = 4.2005p$. As for component $L_R$ will calculated and renamed as $L_1 = 0.2496$ nH. The design will be mirrored creating $C_4 = C_6 = C_1 = C_3$ , $C_2 = C_5$ and $L_2 = L_1$ to increase the control over simulation, Finally , $C_R$ will be calculated and renamed as $C_7 = 0.7226$ pF.

Another capacitance and inductance will be added from both sides of the circuit to simulate the feedline for microstrip structure as $L_{f1}$ and $C_{f1}$ from the right and $L_{f2}$ and $C_{f2}$ from the left. With the values of $L_{f1} = L_{f2} = 0.0124$ nH and $C_{f1} = C_{f2} = 1e^{-6}$ pF.

The circuit in Figure 2 will be simulated using Advanced Design System (ADS) to simulate S-Parameters from 1GHz to 4GHz to visualize the full circuit response. Before simulating on ADS, a microstrip model must be made for simulation in CST STUDIO SUITE for comparison using Figure 3 as reference.
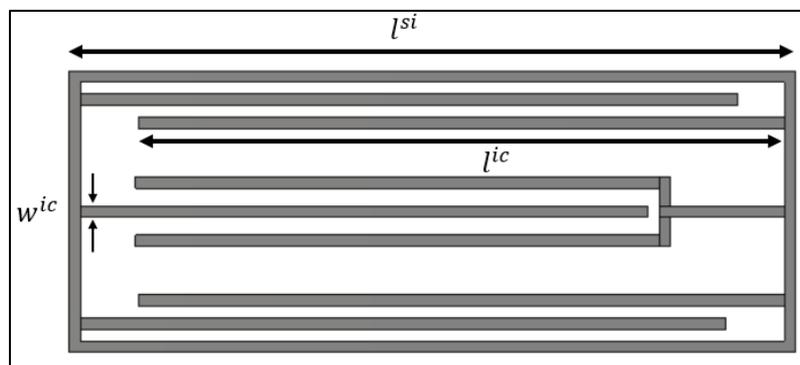


**Fig. 3.** Unit cell of D-CRLH transformer for parameter equations

Using the circuit values mentioned above, the proposed microstrip model in Figure 4 can be realized using Eq. (9) and Eq. (10) mentioned below [1].

$$C_L \cong (\epsilon_r + 1)l^{ic}[(N - 3)A_1 + A_2] \text{ (pF)} \tag{9}$$

For,

$$A_1 = 4.409 \tanh\left[0.55\left(\frac{h}{w^{ic}}\right)^{0.45}\right].10^{-6} \text{ (pF/μm)}$$

$$A_2 = 9.92 \tanh\left[0.52\left(\frac{h}{w^{ic}}\right)^{0.5}\right] . 10^{-6} \quad \left(\frac{pF}{\mu m}\right)$$

$$L_L \cong \frac{Z_c^{si}}{\omega} \tan(\beta^{si} l^{si}) \ (nH) \tag{10}$$

where $Z_c^{si}$, $\beta^{si}$ and $l^{ic}$ represent the characteristic impedance, the propagation constant, and the length of figure. Also $w^{ic}$ and $h$ represent the overall width of its finger and the height of the used substrate. Finally, $l^{ic}$ represents the length of track [1].

A microstrip model will be developed for the proposed circuit using Eq. (9) & Eq. (10), considering the values mentioned for the circuit components. The dimensions of the microstrip model are provided in Table 1.
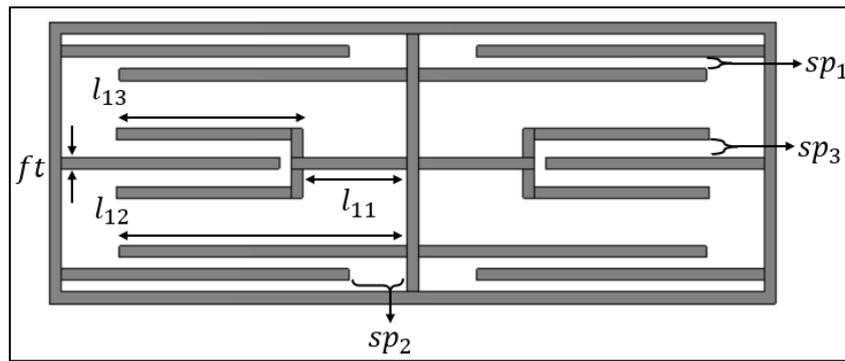


**Fig. 4.** Half-mode D-CRLH unit cell proposed microstrip model on CST

Table 1
Dimensions values of half-mode D-CRLH unit cell

| Label | Dimensions (mm) | Label | Dimensions (mm) |
|---|---|---|---|
| $ft$ | 0.2 | $l_{11}$ | 1.8 |
| $sp_1$ | 0.2 | $l_{12}$ | 4.95 |
| $sp_2$ | 1 | $l_{13}$ | 3.2 |
| $sp_3$ | 0.3 | - | - |

As observed in Figure 5, the insertion loss, symbolled as $S_{21}$, of both simulated ADS and CST model, is observed to have values of approximately 1.2dB for frequency range from 1GHz to 4GHz. To conclude this section, the half-mode D-CRLH unit cell covers the desired wireless bands with no interference.
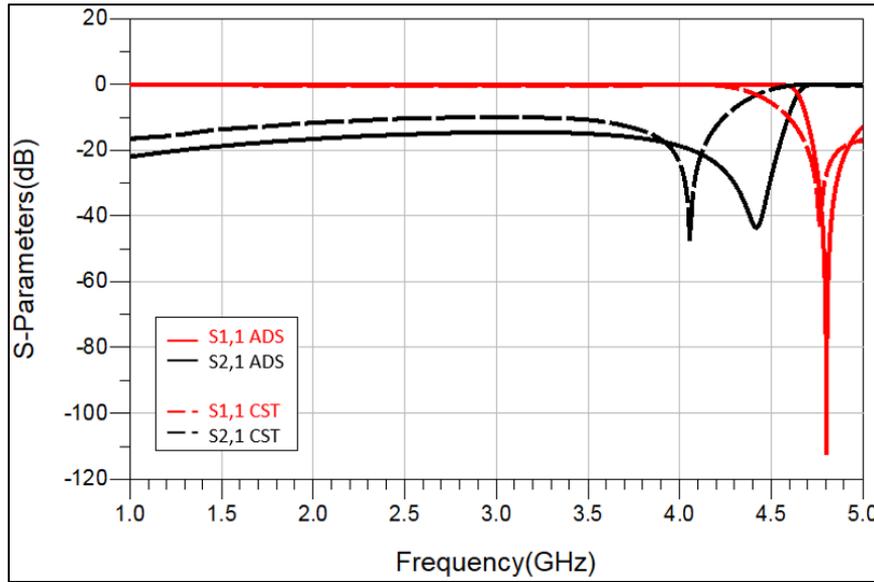
**Fig. 5.** Simulated S-parameters for half-mode D-CRLH unit cell equivalent

In the next section, loads will be applied to the half-mode D-CRLH unit cell, resulting in a loaded D-CRLD unit cell that exhibits duality in frequency bands. To simulate inductance, mender line structures will be used for load application [23], and a metal sheet will be applied at the end to simulate capacitance.

## 2.2. Loaded D-CRLH Transformer

Now that the following has been determined, $C_L = 4.4005p$, $L_R = 0.2496 \, nH$ and $C_R = 0.7226 \, pF$, one can determine the values of $L_L$, using the loaded D-CRLH in Figure 1(a) to deduce the below from Eq. (1). Mentioned above.

$$\cos \beta d = 1 + 0.5 * \frac{(j\omega L_R)\left(\frac{1}{j\omega C_L}\right)}{(j\omega L_R)+\left(\frac{1}{j\omega C_L}\right)} * \frac{1}{(j\omega C_R)+\left(\frac{1}{j\omega L_L}\right)} \tag{11}$$

Solving Eq. (11) for $\beta d = \pi$,

$$\frac{(j\omega L_R)\left(\frac{1}{j\omega C_L}\right)}{(j\omega L_R)+\left(\frac{1}{j\omega C_L}\right)} * \frac{1}{(j\omega C_R)+\left(\frac{1}{j\omega L_L}\right)} = -4 \tag{12}$$

When solving for $\beta d = \pi$ the cut off frequency of the dual bands can be determined. Since it is desired to create notch at 1.8GHz and another at 2.6GHz, separating the two band, $\omega$ will be determined as 0.9GHz, for notch at 1.8GHz, and as 1.3GHz, for notch at 2.6GHz. Since this is being designed for a novel reconfigurable diplexer, the below must be satisfied.

$$Z_o = \sqrt{\frac{Z}{Y}} = \sqrt{\frac{(j\omega L_R)\left(\frac{1}{j\omega C_L}\right)}{(j\omega L_R)+\left(\frac{1}{j\omega C_L}\right)} \Big/ \frac{1}{(j\omega C_R)+\left(\frac{1}{j\omega L_L}\right)}} = 70.7\Omega \tag{13}$$

$$S_{21} = \frac{2}{A+D+(B/Z_o)+(C*Z_o)} = \text{Zero} \tag{14}$$

For,

$$A = 1 + ZY = 1 + \frac{(j\omega L_R)\left(\frac{1}{j\omega C_L}\right)}{(j\omega L_R)+\left(\frac{1}{j\omega C_L}\right)} * \frac{1}{(j\omega C_R)+\left(\frac{1}{j\omega L_L}\right)}$$

$$B = Z = \frac{(j\omega L_R)\left(\frac{1}{j\omega C_L}\right)}{(j\omega L_R)+\left(\frac{1}{j\omega C_L}\right)}$$

$$C = Y = \frac{1}{(j\omega C_R)+\left(\frac{1}{j\omega L_L}\right)}$$

$$D = 1$$

Using Eq. (12), Eq. (13) or Eq. (14), the value of $L_L$ can be calculated as 6.2085 nH, for notch at 1.8GHz, and as 3.4103 nH, for notch at 2.6GHz.

In Figure 6, a detailed circuit for loaded D-CRLH transformers is proposed, providing more control over the simulation by dividing its basic components. Using the circuit in Figure 1(a) as reference.
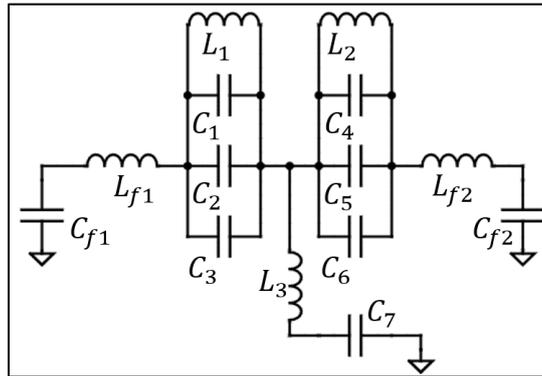


**Fig. 6.** Loaded D-CRLH equivalent circuit

Similar as before, the component $C_L$, calculated as 4.4005pF, will be divide to $C_1 = C_3 = 0.1$ pF and $C_2 = 4.2005p$. As for component $L_R$ and $C_R$ both will be calculated and renamed as $L_1 = 0.2496$ nH & $C_7 = 0.7226$ pF respectively. The design will be mirrored creating $C_4 = C_6 = C_1 = C_3$ , $C_2 = C_5$ and $L_2 = L_1$ to increase the control over simulation.

The component $L_L$ will be renamed as $L_3$ and simulated once for 6.2085 nH, for notch at 1.8GHz, and another for 3.4103 nH, for notch at 2.6GHz.

Another capacitance and inductance will be added from both sides of the circuit to simulate the feedline in microstrip structure as $L_{f1}$ and $C_{f1}$ from the right and $L_{f2}$ and $C_{f2}$ from the left. With the values of $L_{f1} = L_{f2} = 0.0124$ nH and $C_{f1} = C_{f2} = 1e^{-6}$ pF.

Prior to simulating the circuit in Figure 6 with Advanced Design System (ADS) to visualize S-parameters from 1GHz to 4GHz, a microstrip model Figure 7(a) & (b) was constructed for simulation in CST STUDIO SUITE. This model is based on Eq. (9) & Eq. (10) from the previous section.
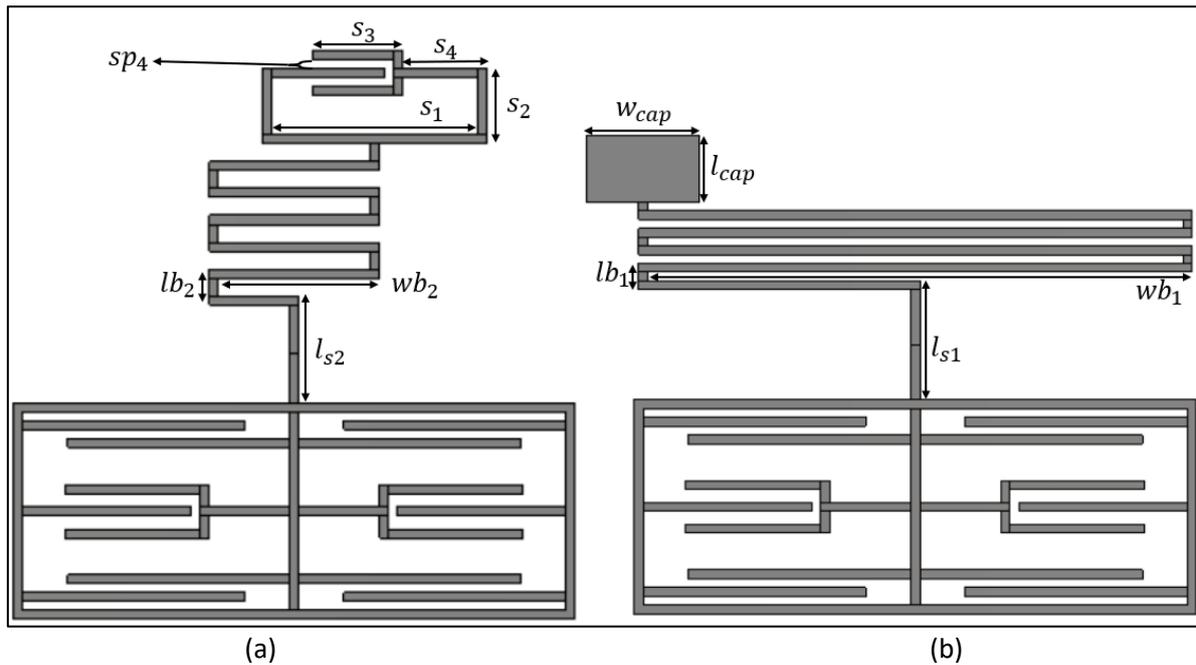
**Fig. 7.** Proposed loaded D-CRLH unit cell with (a) Load to create notch at 2.6GHz & (b) Load to create notch at 1.8GHz

**Table 2**
Values of loaded half-mode D-CRLH unit cell in figure 6(a) & (b)

| Label | Dimensions (mm) | Label | Dimensions (mm) | Label | Dimensions (mm) |
|---|---|---|---|---|---|
| $l_{s1}$ | 2.5 | $l_{s2}$ | 2.5 | $s_3$ | 1.8 |
| $wb_1$ | 12.5 | $wb_2$ | 4.5 | $s_4$ | 1.7 |
| $lb_1$ | 0.6 | $lb_2$ | 0.8 | $sp_4$ | 0.2 |
| $l_{cap}$ | 1.5 | $s_1$ | 4.6 | | |
| $w_{cap}$ | 2.5 | $s_2$ | 1.5 | | |

As observed in Figure 8(a), the insertion loss $S_{21}$, of both simulated ADS and CST models, is observed to have values of approximately 1.3dB for frequency range from 1GHz to 4GHz with a notch at 2.6GHz having a suppression band of 300MHz. Similar for Figure 8(b), the insertion loss $S_{21}$, of both simulated ADS and CST models, is observed to have values of approximately 1.2dB with a notch at 1.8GHz having a suppression band of 300MHz.
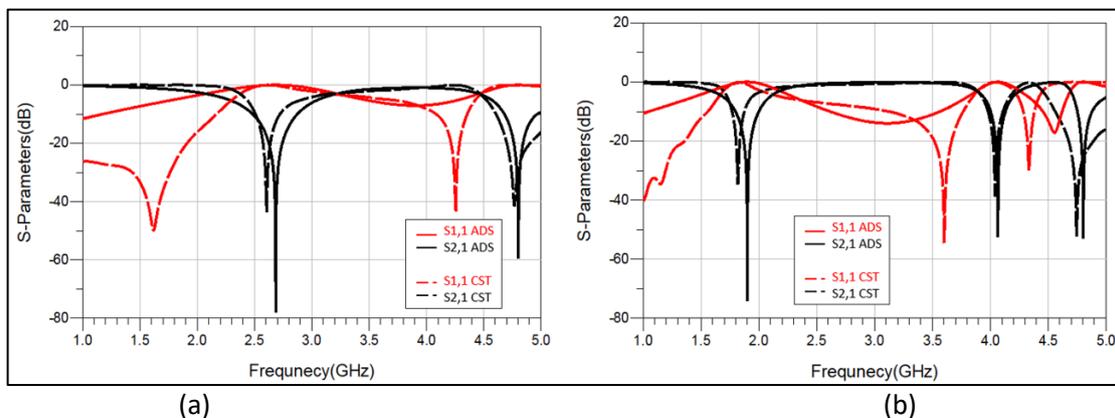


**Fig. 8.** Simulated S-parameters on ADS and CST for (a) Loaded D-CRLH unit cell with load to create notch at 2.6GHz & (b) Loaded D-CRLH unit cell with load to create notch at 1.8GHz

In the next section, an RF switch will be inserted in the load line of the unit cell, enabling the alteration of the response between the loaded and half-mode D-CRLH transformer. This configuration achieves reconfigurability in the system.

## 2.3. Reconfigurable Loaded D-CRLH Transformer

The chosen PIN diode for the proposed design is the Silicon PIN-Diode BAR 64 by Infineon Technologies AG. This diode is suitable for radio frequency attenuators and switches and operates in the frequency range of 1MHz to 6GHz [24]. The equivalent circuit for biasing the PIN diode is shown in Figure 9.
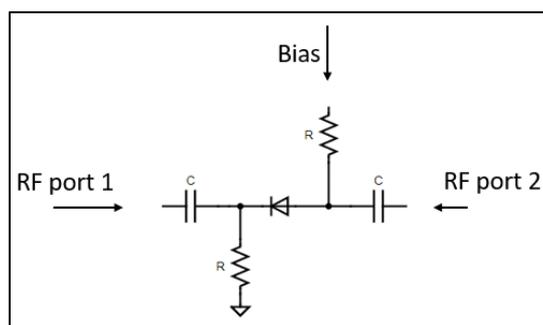


**Fig. 9.** Equivalent circuit for biasing the PIN-diode switch

It functions as a high voltage current-controlled RF resistor, enabling the control of large RF signals with lower current levels. Also, Figure 10(a) & (b) shows the section of which the PIN diode will be attached to load line.
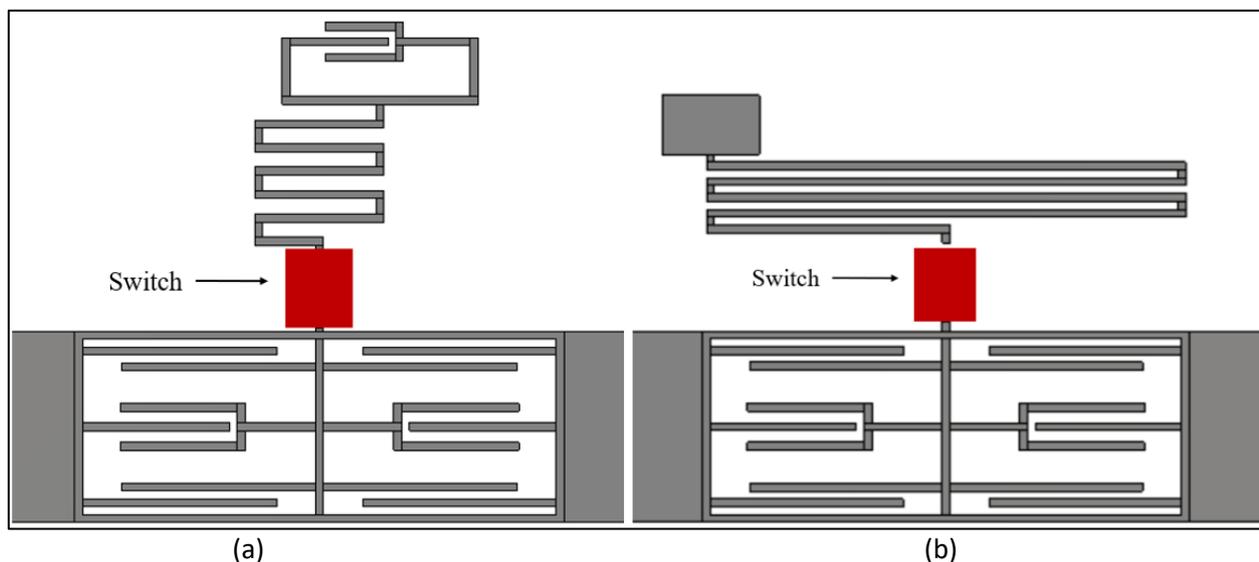


(a)  (b)

**Fig. 10.** 2D Layout of loaded D-CRLH transformer with removed loaded line for (a) Load to create notch at 2.6GHz & (b) Load to create notch at 1.8GHz

To provide proof of concept of the recognizability property, a simulation will be conducted on Loaded D-CRLH equivalent circuits via ADS, with an addition section which simulates the ON and OFF state of the PIN-Diode switch, this can be seen in Figure 11(a) & (b).

Similar to the above section, the values of the Loaded D-CRLH equivalent circuits will remain the same, with respect to the values of load line to create a notch at 2.6GHz and 1.8GHz with both having a suppression band of 300MHz, with the addition of $L_{OFF} = 0.6\,\mu H$, $R_{OFF} = 3K\Omega$ and $C_{OFF} = 0.17pF$, as shown in Figure 11(a), to simulate the PIN-Diode in OFF state, while the addiction of $L_{ON} = 0.6\,\mu H$ and $R_{ON} = 2.1\Omega$, as shown in Figure 11(b), to simulate the PIN-Diode in ON state.

Another simulation will be conducted on Loaded D-CRLH Transformer microwave structures in Figure 10(a) & (b), to simulate the states of the PIN-Diode a variable resistance will be placed between the load line and the Loaded D-CRLH Transformer, at its maximum value the load line will be disconnected thus achieving reconfigurability.
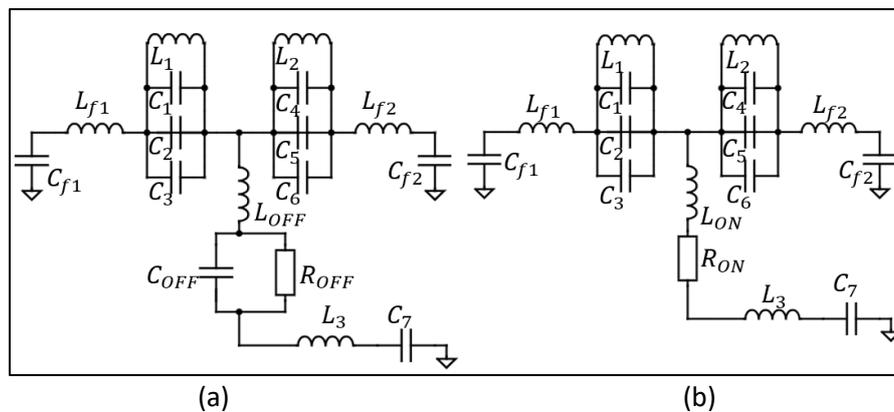


(a)                                                    (b)

**Fig. 11.** Loaded D-CRLH equivalent circuit with PIN-Diode equivalent circuit in (a) OFF state and (b) ON state



(a)                                                    (b)

**Fig. 12.** (a) Simulation of loaded D-CRLH equivalent circuit to create notch at 2.6GHz Via ADS in both states of PIN-Diode switch and (b) Simulation of loaded D-CRLH microstrip structure to create notch at 2.6GHz Via CST in both states of PIN-Diode switch
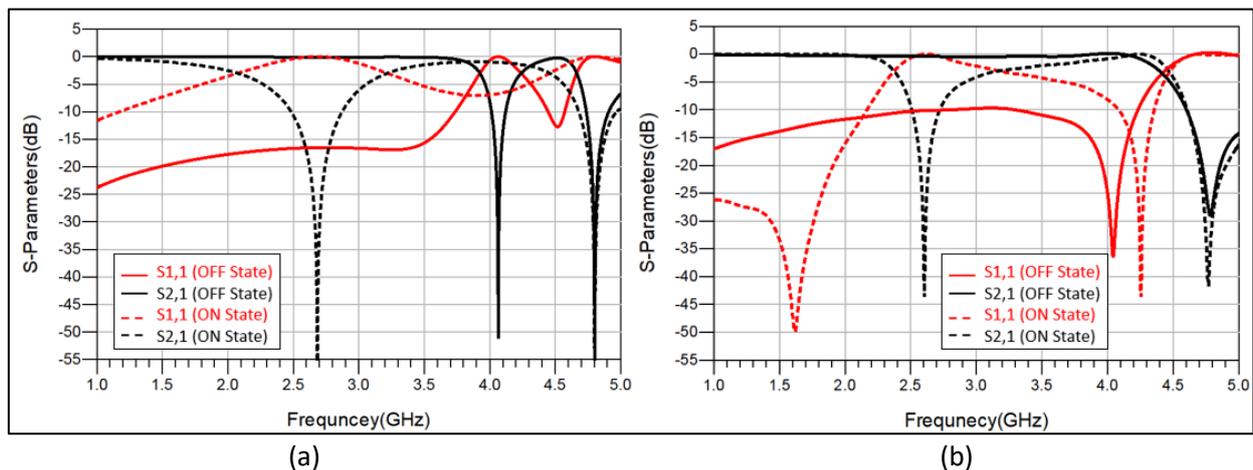
**Fig. 13.** (a) Simulation of loaded D-CRLH equivalent circuit to create notch at 2.6GHz via ADS in both states of PIN-Diode switch and (b) Simulation of loaded D-CRLH microstrip structure to create notch at 2.6GHz via CST in both states of PIN-Diode switch
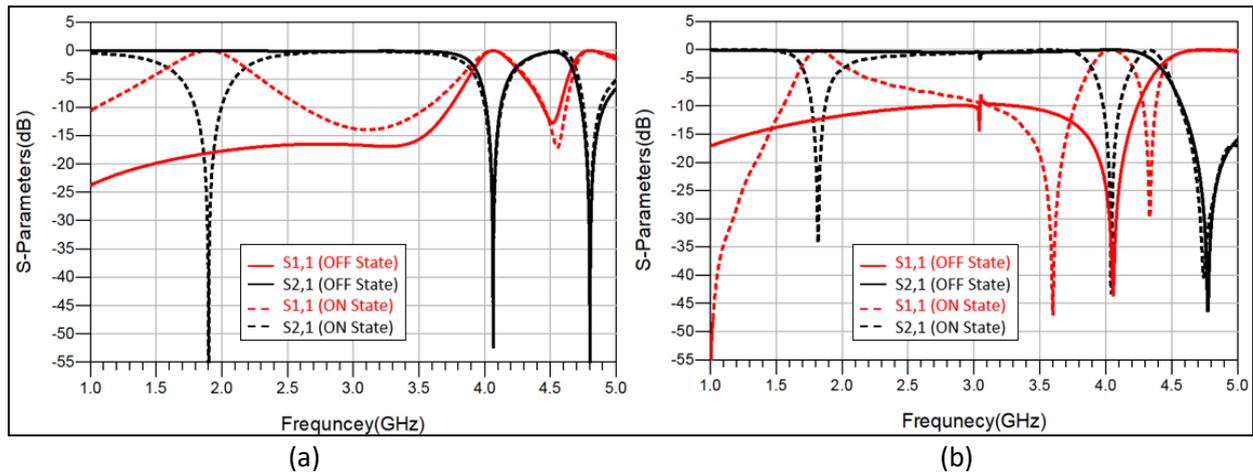
Upon careful examination of both Figure 12(a) and (b), as well as Figure 13(a) and (b), it becomes evident that the reconfigurability property is discernible not only at the equivalent circuit level but also at the microwave structure level. These observations suggest that the capability for reconfiguration is embedded in both the underlying circuitry and the larger microwave architecture.

The next section of the discussion is poised to introduce the Proposed Novel Reconfigurable Diplexer. Within this section, not only will the diplexer itself be presented, but also the results derived from simulation and the outcomes of the fabrication process. This comprehensive approach aims to provide a holistic view of the diplexer's performance, validating its reconfigurable nature at both the theoretical and practical levels.

## 3. Simulation and Measurement of Proposed Novel Reconfigurable Diplexer

The two loaded D-CRLH transformers will be combined into a single design, giving the proposed novel reconfigurable diplexer, with two ports operating at frequency range of 1GHz to 4GHz with the ability to cancel out 1.8GHz and 2.6GHz with suppression band of 300MHz by turning ON the PIN-diode switch placed at the load line as shown in both Figure 10(a) & (b).

The novel reconfigurable diplexer was designed using CST STUDIO SUITE on a dielectric substrate (Roger RT5880) with $\varepsilon_r$= 2.2 and thickness of 1.575mm within a total area of $39x15\text{mm}^2$. The designed diplexer has a characteristic impedance of 50Ω, the diplexer design can be seen in Figure 14 along with the calculated dimensions mentioned in Table 3.
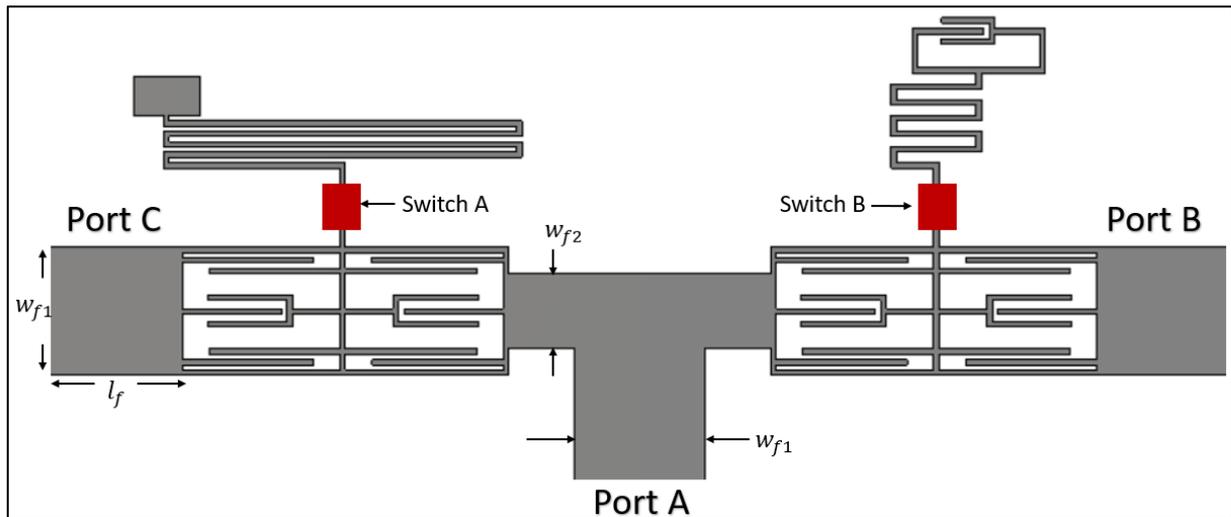
**Fig. 14.** Proposed novel reconfigurable diplexer

Table 3
Proposed novel reconfigurable diplexer dimensions

| Label | Dimensions (mm) |
|---|---|
| $l_f$ | 5 |
| $w_{f1}$ | 4.871 |
| $w_{f2}$ | 2.815 |

The values of $w_{f1}$ and $w_{f2}$ were determined based on their characteristic impedance with $w_{f1}$ having a characteristic impedance of 50Ω and $w_{f2}$ having a characteristic impedance of 70.7Ω.

The proposed novel reconfigurable diplexer will function as low pass filter, the input signal will enter from Port A and then be divided and filtered through Port B and Port C.

The proposed novel reconfigurable diplexer was fabricated on a on a dielectric substrate (Roger RT5880) with $\varepsilon_r$= 2.2 and thickness of 1.575mm within a total area of $39x15mm^2$, The S-Parameters are measured of real fabrication by Rohde & Schwarz ZVL20 network analyser. Figure 15(a) shows fabricated diplexer without switches.



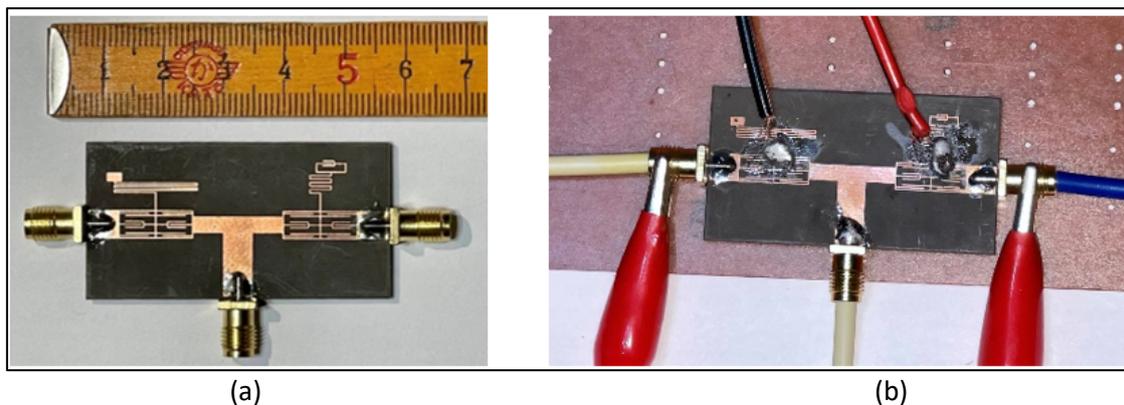(a)                                                   (b)

**Fig. 15**. (a) Fabricated novel reconfigurable diplexer without PIN-Diode switches, (b) fabricated novel reconfigurable diplexer with PIN-Diode switches connected to Rohde & Schwarz ZVL20 network analyser

The proposed diplexer is designed to be reconfigurable , thus a section of the load line was removed and Silicon PIN Diode BAR 64 by Infineon Technologies AG is applied. The proposed diplexer then was connected to Rohde & Schwarz ZVL20 network analyser and evaluated all switch modes.
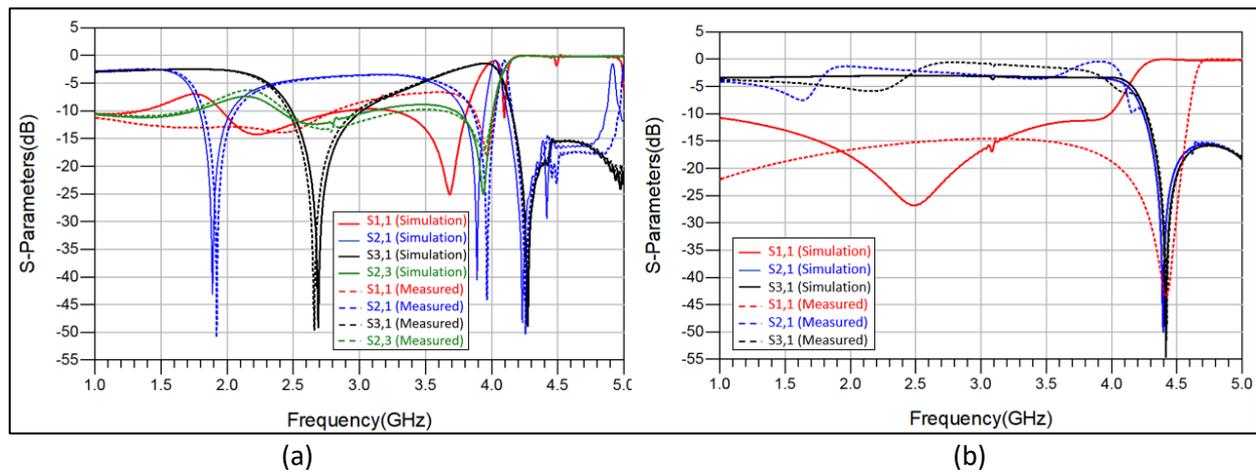


**Fig. 16**. Simulated and measured insertion and isolation responses with (a) PIN-Diode switch ON of Port B & Port C & (b) PIN-Diode switch OFF of Port B & Port C

When observing Figure 16(a), one can observe that the insertion loss of both simulated and measured at Port B, $S_{21}$, both having an average value of 3.2dB then increases at centre frequency 1.8GHz, thus suppressing the mentioned band with bandwidth of 300MHz. Similarly, the insertion loss of both simulated and measured at Port C, $S_{31}$, both having an average value of 3.2dB then increases at centre frequency 2.6GHz with suppression bandwidth of 300MHz.

As for Figure 16(b), it is observable that both simulated and measured responses for both Ports when the PIN-Diode switch is OFF are the same with no harmonics and both having an insertion loss of 3.2dB, thus archiving reconfigurability.

## 4. Conclusions

An efficient structure of microstrip novel reconfigurable diplexer based on D-CRLH metamaterial technique is introduced that supports a wide frequency band from 1GHz to 4GHz, covering a wide range of wireless applications, with it being reconfigurable with notches to cantered at bands 1.8GHz and 2.6GHz with both notches having suppression bandwidth of 300MHz.

**Table 4**
Comparison between the proposed novel reconfigurable diplexer and previously reported diplexers

| Reference | Dimensions (mm$^2$) | Dimensions($\lambda_g{}^2$) | Insertion Loss of Unit Cell (dB) | Center Frequency (GHz) |
|---|---|---|---|---|
| [18] | 65 x 25 | 0.79 x 0.30 | 1.7 | 2.5 |
| [21] | 12.9 x 3.5 | 0.19 × 0.05 | 1.2 ~ 1.6 | 2.4/3.5 |
| [21] | 23.1 x 4 | 0.34 × 0.06 | 1.55 ~ 1.85 | 2.4/3.2 |
| [22] | 30 x 60 | 0.52 × 1.14 | 1 ~ 1.2 | 2.1 / 2.6 |
| This Work | 39 x 15 | 0.34 x 0.13 | 1.2 ~ 1.3 | 2 |

As seen in the Table 4, The design presents a novelty in size structure for a reconfigurable microstrip diplexer as the structure measured by a compact dimension 39x15 mm$^2$ with reasonable

response values. Finally, the results of S-Parameters were measured by Rohde and Schwarz-ZVL20 Network tester which presents an excellent matching with the results of simulation and the equivalent circuit results.

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