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A Predictive Approach to Reduce Intrinsic Gate Delay in Junctionless Double Gate Strained Transistor using DoE-Based Genetic Algorithm

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ABSTRACT

The aim of reducing the size of a transistor is not only to compress more transistors into a denser area and increase switching speed, but also to reduce the intrinsic gate delay. This paper introduces a predictive approach to reduce intrinsic gate delay in Junctionless Double Gate Strained Transistor (JLDGST). The study involves 2D simulation and a hybrid Multiple Regression Analysis – Genetic Algorithm (MRA-GA) model for device simulation and optimization respectively. Initially, 18 sets of experiment are employed for obtaining multiple magnitude of intrinsic gate delay. Based on the retrieved results, the objective function that relates multiple input parameters (Ge mole fraction, high-*k* material thickness, source/drain doping concentration and metal work-function) with the output response (intrinsic gate delay) is derived using MRA. The derived objective function is then utilized as an input to the GA for searching the local minima of the fitness function. The final result shows that the proposed hybrid MRA-GA model has significantly reduced the intrinsic gate delay of the device by approximately 70%. The most optimum magnitude of Ge mole fraction, $T_{high\text{-}k}$, N_{sd} and WF for the lowest possible intrinsic gate delay of the JLDGST are predicted to be 0.3 (30%), 3 nm, 2.96×10^{13} cm^{-3} and 4.6 eV respectively.

Keywords:

Genetic algorithm; Intrinsic gate delay; JLDGST; Multiple regression analysis

1. Introduction

Intrinsic gate delay is a crucial transistor's characteristic contributed due to the internal capacitances which is normally influenced by the geometrical and process parameters of the transistor especially in nano-scale regime. The intrinsic gate delay (τ_{int}) of a transistor is the time it takes for a transistor's gate voltage to reach a given threshold level and then switch the transistor between the ON and OFF states. It is a crucial parameter in digital circuits due to the way it affects the circuit's overall efficiency and efficacy. The primary factor that affects the intrinsic gate delay is

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how the parasitic capacitances of the transistor's gate and the load capacitance linked to the output of the gate charge and drain. The gate delay is affected by the capacitance of the load connected to the output of the gate. Larger capacitance of the load necessitates more time to charge or discharge, resulting in a longer gate delay. Reducing the capacitance of the load may be useful in decreasing the intrinsic gate delay.

Kumar *et al.,* [1] reported that the optimization in geometrical and process parameters of gate-all-around transistor caused the rate of increase of drain current to be dominated by the increase in the device's intrinsic capacitance, thereby reducing the intrinsic gate delay. The optimized device reduced the optimal gate delay from 8.5 to 6.3 psec. Seifollahi *et al.,* [2] reported that the variation in gate length of double-gate FET has a substantial effect on intrinsic gate delay, with the optimized device exhibiting the lowest intrinsic delay time recorded at 0.442 psec. According to Ryu *et al.,* [3], the increased spacer area reduces the parasitic capacitance. With a 1nm-wide silicon nitride spacer material, the device's performance was optimized, and the smallest intrinsic delay time recorded was approximately 0.3 psec. Yiming Li *et al.,* [4] reported that work function variations had a substantial effect on the intrinsic gate delay caused by load capacitance fluctuations. With an increasingly work-function value, the Vth of the N-type gate-all-around FET increases, and it becomes more difficult to turn on the device, resulting in a longer intrinsic gate delay. Jegadheesan *et al.,* [5] reported that when narrower nanosheets are utilized, the intrinsic latency increases marginally due to a reduction in on-current (I_{ON}). For varying nanosheet width from 10 to 24 nm, a maximum delay reduction of 15% is observed, and for increasing nanosheet width from 24 to 50 nm, a delay reduction of approximately 10% is observed. Avila *et al.,* [6] reported that the gate length and fin spacing have a significant impact on the intrinsic gate latency in FinFET technology. The observations indicate that the parasitic gate resistance has a significant impact on the performance of the circuit.

Based on the aforementioned literatures, it is evident that variations in geometrical and process parameters had a significant effect on the intrinsic gate delay of all transistor types. Numerous researches on application of optimization approaches have been conducted to improve the performances of semiconductor devices [7-9]. Design of experiments (DoE) have been widely utilized to assists designers to model the design parameters of the semiconductor devices and other engineering fields in conjunction with its desired performance [10-17]. Therefore, this paper will introduce a predictive and comprehensive approach for modelling multiple design parameters of Junctionless Double Gate Strained Transistor (JLDGST) for lower intrinsic gate delay using a DoE-based genetic algorithm. The novel contributions of this research work are listed as below:

i. A proposed predictive and systematic approach using a design of experiments (DoE)-based genetic algorithm was introduced.
ii. The impact of design parameters of JLDGST device towards intrinsic gate delay was systematically analysed and studied. The analysis showed that metal work-function was the most significant design parameter contributing the considerable variance on the intrinsic gate delay.
iii. The optimal design parameters of the JLDGST device that produced the lowest possible intrinsic gate delay were optimized and predicted. The intrinsic gate delay was successfully reduced by approximately 70%.

2. Methodology

2.1 2D Simulation

2D simulation for n-type junctionless double-gate strained transistor (JLDGST) was performed by using Silvaco TCAD tools. The 2D simulation was carried out using two separate modules in which the process and device simulation were conducted using Athena and Atlas module respectively. The process simulation flow for the device is depicted in Figure 1.

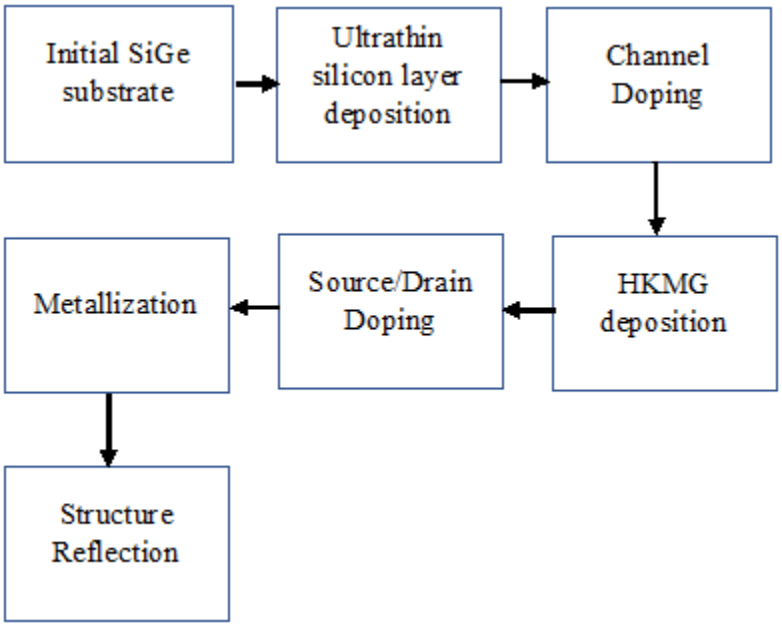

Fig. 1. Process simulation flow for n-type JLDGST [18]

The main substrate of the device was silicon germanium (SiGe) with the initial Ge mole fraction of 0.2 (20%). A very thin Si film with thickness of 1 nm was then deposited on the top of the SiGe substrate in order to form a tensely strained channel. Next, the strained body was doped with high Arsenic concentration of 1 x 10^{17} cm^{-3} for n^+ region formation. The process was then followed by HKMG formation in which the Hafnium dioxide (HfO_2) and Tungsten silicide (WSi_x) were used as a high-*k* dielectric insulator and metal-gate respectively [19]. The thickness of Hafnium dioxide (HfO_2) and work-function of the metal-gate (WSi_x) were initially set at 2 nm and 4.7 eV respectively. Subsequently, the side of the substrate body was considerably doped with 2 x 10^{13} cm^{-3} of Arsenic concentration for n region formation. Both channel and S/D region were doped with same polarity dopant (Arsenic) in order to form junctionless configuration (n - n^+- n). After that, Aluminium was sputtered on the surface of the structure and subsequently etched to form contact for S/D regions. Lastly, the cross-sectional structure of the n-type JLDGST was completed by reflecting the left *x*-axis and upper y-axis as shown in Figure 2. The initial magnitude of the design parameters of the device were summarized in Table 1.

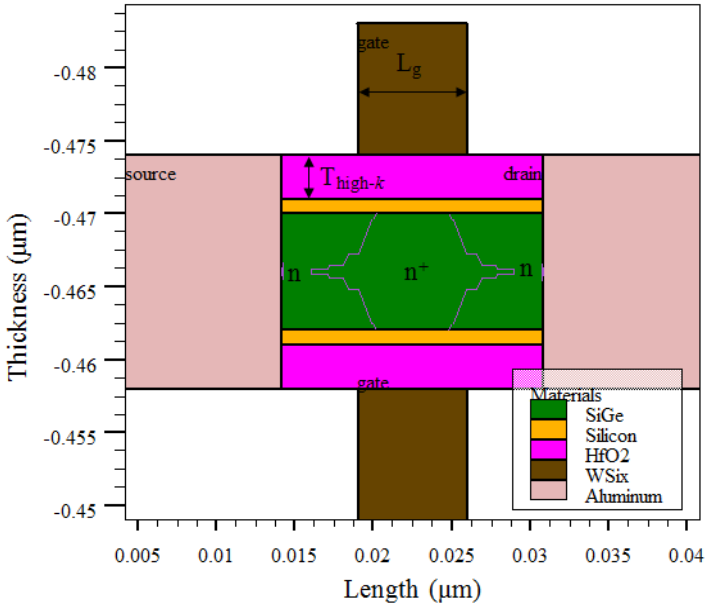

Fig. 2. Cross-sectional structure of n-type JLDGST

After the device structure was completed through Athena module, the structure file was used as an input of the Atlas module for extracting the related device characteristics. AC small signal analysis was conducted to extract the intrinsic capacitances (C_{int}) by supplying an input AC frequency (f) of 1 MHz as the gate-to-source voltage (V_{gs}) was swept from 0 V to 1 V at a constant drain-to-source voltage (V_{ds}) of 0.5 V. The intrinsic capacitances (C_{int}) of the JLDGST can be measured by summing up the magnitude of gate-to-source capacitance (C_{gs}) and gate-to-drain capacitance (C_{gd}), mathematically expressed as:

$$C_{\text{int}} = C_{gs} + C_{gd} \tag{1}$$

Table 1
Initial magnitude of design parameters for n-type JLDGST

Design Parameters	Units	Magnitude
Ge mole fraction in SiGe layer	-	0.2 (20%)
High-*k* material Thickness, $T_{high\text{-}k}$	nm	2
S/D Doping, N_{sd}	cm^{-3}	2.0E13
Metal Workfunction (WF)	eV	4.7

Figure 3 depicts the plot of C_{int}-V_{gs} at a constant V_{ds} = 0.5 V as the the V_{gs} is shifted from 0 V to 1 V. It is observed that the magnitude of C_{int} is increased as the V_{gs} is biased towards maximum. The increase in C_{int} magnitude becomes more prominent as the device operates in saturation mode. Theoretically, the larger C_{int} magnitude would result in higher intrinsic gate delay (τ_{int}) as mathematically described by:

$$\tau_{\text{int}} = \frac{C_{\text{int}} \times V_{DD}}{I_{ds}} \tag{2}$$

However, intrinsic gate delay for n-type JLDGST is still heavily depended on the drain current (I_{ds}) due to its large magnitude. Since the I_{ds} is inversely proportional with the delay, large number of induced I_{ds} would dominantly govern the delay over the C_{int} variation. Figure 4 depicts the initial plot of τ_{int}-V_{ds} at a constant V_{gs} = 0.5 V as the the V_{ds} is shifted from 0 V to 1 V. Based on the plot, it can be observed that the intrinsic gate delay of the device is directly proportional to the V_{ds} as the delay tremendously increases as a higher V_{ds} is supplied. The initial magnitude of the intrinsic gate delay of the device at a maximum V_{ds} (1V) is measured to be 5.6 psec. In the subsequent sections, the design parameters (Ge mole fraction, $T_{high\text{-}k}$, N_{sd} and WF) will be predictively optimized for much lower intrinsic gate delay using a MRA-GA model.

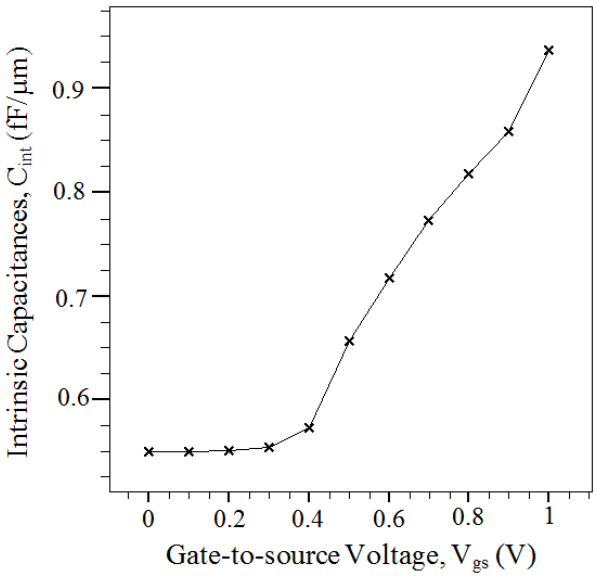

Fig. 3. Plot of C_{int}-V_{gs} transfer characteristic

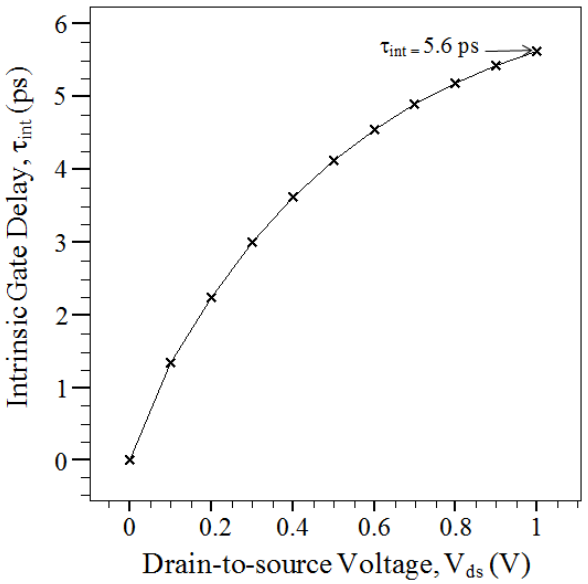

Fig. 4. Plot of τ_{int}-V_{ds} transfer characteristic

2.2 Predictive Optimization using DoE-Based Genetic Algorithm

The optimization process of the n-type JLDGST was conducted using a hybrid Multiple Regression Analysis – Genetic Algorithm (MRA-GA) predictive model. The proposed model comprised two stages known as Multiple Regression Analysis (MRA) and Genetic Algorithm. Figure 5 shows the general flowchart of the predictive optimization using a hybrid MRA-GA model.

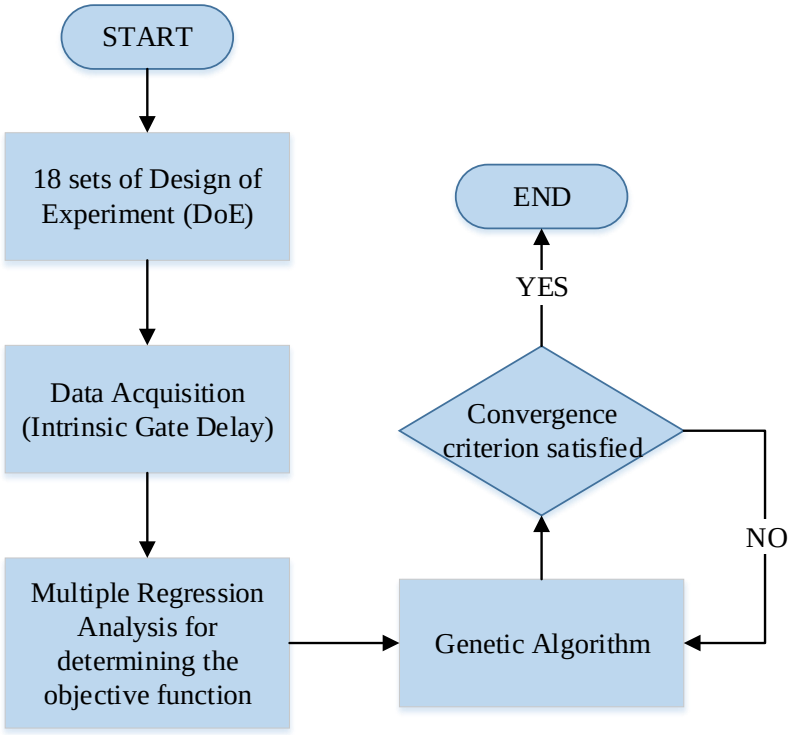

Fig. 5. General flowchart of a hybrid MRA-GA predictive optimization

2.2.1 Multiple regression analysis (MRA)

Multiple Regression Analysis (MRA) is one of many types of linear regression analysis. As a predictive approach, the MRA is often utilized to express the relationship between one continuous dependent output and two or more independent inputs [20-24]. In this study, a continuous dependent output is the intrinsic gate delay (τ_{int}) denoted by *y* while the four independent inputs are Ge mole fraction, $T_{high\text{-}k}$, N_{sd} and WF denoted by x_1, x_2, x_3 and x_4 respectively. The independent inputs are varied into three multiple levels in order to design 18 sets of experiment. The independent inputs with multiple levels and the design of experiment (DoE) involved in this study are shown in Table 2 and Table 3 respectively.

Table 2
Independent inputs with multiple levels

Symbol	Parameter	Unit	Level		
			Low	Medium	High
x_1	Ge mole fraction in SiGe layer	-	0.1 (10%)	0.2 (20%)	0.3 (30%)
x_2	High-k material Thickness, $T_{high\text{-}k}$	nm	1	2	3
x_3	S/D Doping, N_{ch}	cm^{-3}	$1x10^{13}$	$2x10^{13}$	$3 x10^{13}$
x_4	Metal Workfunction (WF)	eV	4.6	4.7	4.8

The multiple regression equation that includes four independent inputs (x_1, x_2, x_3 and x_4) and one dependable output can be expressed as:

$$Y = a + b_1x_1 + b_2x_2 + b_3x_3 + b_4x_4 + e \quad (3)$$

where *a* is the intercept, $b_1b_2b_3b_4$ is the regression coefficients and *e* is the error term. Based on Table 3, the relationship between the inputs, output and their corresponding coefficients can be written in generalized matrix form as:

$$\begin{pmatrix} y_1 \\ y_2 \\ \vdots \\ y_n \end{pmatrix} = \begin{pmatrix} x_{11}\ x_{12}\ x_{13}\ x_{14} \\ x_{21}\ x_{22}\ x_{23}\ x_{24} \\ \vdots \\ x_{n1}\ x_{n2}\ x_{n3}\ x_{n4} \end{pmatrix} \begin{pmatrix} a \\ b_1 \\ \vdots \\ b_4 \end{pmatrix} + \begin{pmatrix} e_1 \\ e_2 \\ \vdots \\ e_n \end{pmatrix} \tag{4}$$

where *n* is the number of matrix rows which are 18. In order to estimate the regression coefficients, the error term (e) will be neglected. Hence, the corresponding magnitude of a, b_1, b_2, b_3, b_4 can be determined by solving the matrices. Finally, the objective function based on the multiple regression model can be derived as:

$$Y' = a + b_1x_1 + b_2x_2 + b_3x_3 + b_4x_4 \tag{5}$$

Table 3
18 sets of design of experiment

No.Exp.	x_1	x_2 (nm)	x_3 (x10^{13})	x_4 (eV)	y (ps)
1	0.1	1	1	4.6	3.8
2	0.1	1	1	4.7	11
3	0.1	1	2	4.8	57.8
4	0.1	2	2	4.6	2.4
5	0.1	2	3	4.7	5.1
6	0.1	2	3	4.8	25.5
7	0.2	3	1	4.6	3
8	0.2	3	1	4.7	5.7
9	0.2	3	2	4.8	13.7
10	0.2	1	2	4.6	2.6
11	0.2	1	3	4.7	6.1
12	0.2	1	3	4.8	43
13	0.3	2	1	4.6	2.9
14	0.3	2	1	4.7	6.6
15	0.3	2	2	4.8	24.1
16	0.3	3	2	4.6	2
17	0.3	3	3	4.7	3.1
18	0.3	3	3	4.8	9.3

2.2.2 Genetic algorithm

Genetic algorithm (GA) is a heuristic search-based predictive optimization that is inspired by natural evolution. It is commonly utilized to generate the most optimal or near-optimal solutions to numerous complicated problems [25-29]. The working principle of GA is fundamentally based on a population of chromosomes that act as a set of multiple solutions to the specific optimization problems. In the process of a generation of a population, the chromosomes are randomly kept changed for newly better chromosomes with higher evaluation scores. Predictive approach using GA requires multiple subsequent steps consists of initial population, objective function, fitness scaling, selection, crossover and mutation as depicted in Figure 6.

In this case, the initial population was the initial magnitude of the Ge mole fraction, $T_{high\text{-}k}$, N_{sd} and WF which were previously stated in Table 1. Based on the 18 sets of DoE, the objective function was derived by using MRA as described in previous section. Next, the derived objective function was scaled to fit within a specific pre-determined lower and upper boundary called the fitness function (f_i). Since the optimization problem was to search the least possible magnitude of the intrinsic gate delay (τ_{int}), the fitness function (f_i) for this particular problem can be written as:

Minimize $f(x_1, x_2, x_3, x_4)$
Subject to the constraints:
$0.1 \leq x_1 \leq 0.3$
$1 \leq x_2 \leq 3$
$1 \leq x_3 \leq 3$
$4.6 \leq x_4 \leq 4.8$

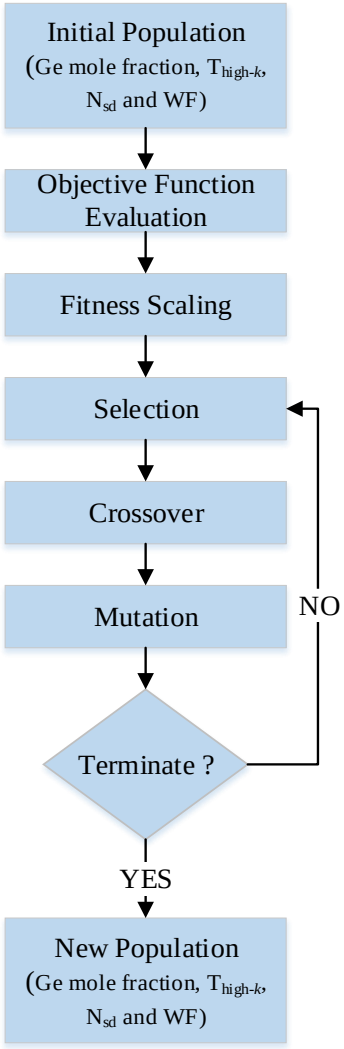

Fig. 6. Flowchart of the Genetic Algorithm

Selection is a process to select a part of the existing population in order to foster a new generation. In this case, each individual solution was selected via a process in which a fitter solution measured by the fitness function was more preferably to be selected. The subsequent step was to

perform crossover in which the genes from the parent chromosomes was opted to form a new offspring. Next step was to perform mutation in order to prevent descending all the possible solutions in population into local optimum of the solved problem. The process of selection, crossover and mutation were repeated until there is no further improvement on the fitness magnitude for certain preset number of generations. The final magnitude of the fitness function was identified at this point, implying that the iterations had been terminated. As a result, the new populations (Ge mole fraction, $T_{high\text{-}k}$, N_{sd} and WF) that generate the best fitness magnitude will be successfully predicted. The GA preferences for this particular study were set as:

Type = real-valued
Population size = 50
Number of generations = 1000
Elitism = 2
Crossover probability = 0.8
Mutation probability = 0.1

3. Results and Discussion

In this section, the results of the predictive optimization for τ_{int} of the JLDGST, involving both MRA and GA approaches will be discussed. After processing all the associated magnitudes of both dependent and independent variables using MRA, the multiple regression plots of the τ_{int} for 18 experimental rows were generated as shown in Figure 7.

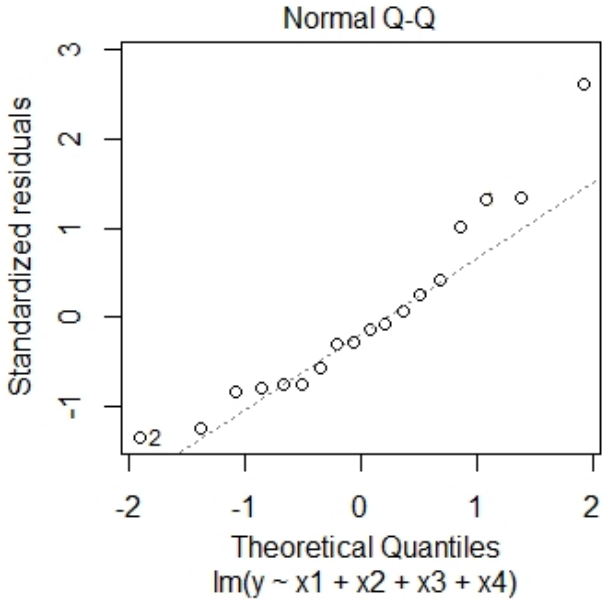

Fig. 7. Multiple Regression plots for Intrinsic Gate Delay (τ_{int})

The final results of the multiple regression analysis (MRA) are summarized in Table 4. According to the estimated regression coefficients (a, b_1, b_2, b_3, b_4) in column 2 of Table 4, the objective function of this study can be relationally expressed as:

$$Y = -630.956 - 15.389x_1 + 6.522x_2 - 2.139x_3 + 141.278x_4 \quad (6)$$

Table 4
Results of the Multiple Regression Analysis

Regression Coefficients	Estimation	Std. Error	t value	Pr (>|t|)	Significant code
Intercept	-630.956	158.61	-3.98	0.0016	**
x_1	-15.389	34.420	-0.45	0.6622	
x_2	-6.522	3.442	-1.9	0.0806	.
x_3	-2.139	3.442	-0.62	0.5451	
x_4	141.278	34.420	4.1	0.0012	**
Significant Code: 0 '***', 0.001 '**', 0.01 '*', 0.05 '.' 0.1-1 ' '					

It is shown that the most independent variables that contribute significant impact on the objective function are intercept and x_4 statistically due to their least Pr (>|t|). Hence, it can be concluded that metal work-function (WF) is the most dominant design parameter influencing the variation in intrinsic gate delay. Based on the specified upper and lower boundaries, the objective function is converted into a fitness function for searching the global minimum. The search of the global minimum finished after 504 generations as the optimum fitness magnitude was found. The plot of the fitness magnitude as the number of generations focalize at the most optimum point are depicted in Figure 8.

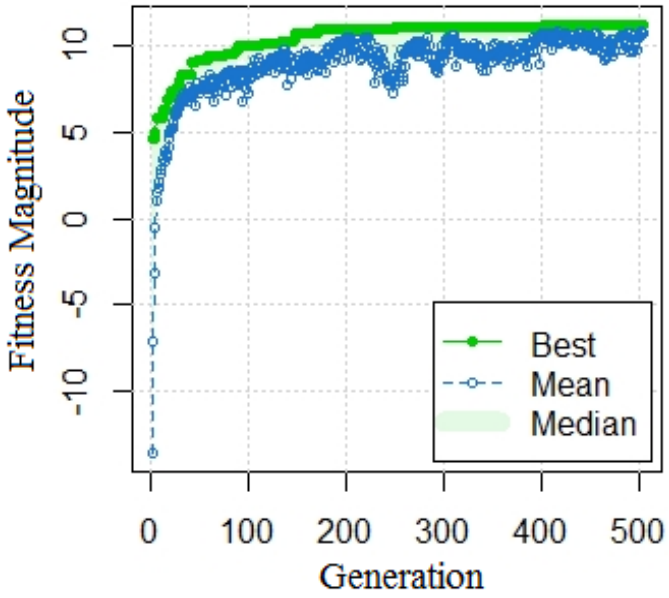

Fig. 8. Performance of GA during convergence

The most optimum design parameters that yield the lowest intrinsic gate delay were successfully predicted by the GA as summarized in Table 5. The highest possible fitness magnitude is measured to be at 11.26682. Since the previous 18 sets of DoE does not comprise the predicted optimum design parameters (Ge mole fraction = 0.29, $T_{high\text{-}k}$ = 3 nm, N_{sd} = 2.96 x 10^{13} cm^{-3} and WF = 4.6 eV), the device simulation needs to be repeated for validation purpose.

Table 5
Summary of the final results of Genetic Algorithm

Parameters	Magnitude and its unit
Fitness Magnitude	11.26682
Ge mole fraction in SiGe layer	0.29 (29%)
High-k material Thickness, $T_{high\text{-}k}$	3 nm
S/D Doping, N_{ch}	2.96 x 10^{13} cm^{-3}
Metal Workfunction (WF)	4.6 eV

After running the device simulation with the predicted design parameters, the τ_{int}-V_{ds} curve is generated and compared to the initial curve as depicted in Figure 9. It is shown that the intrinsic gate delay (τ_{int}) of the n-type JLDGST is deducted for approximately 70% after applying the predictive optimization.

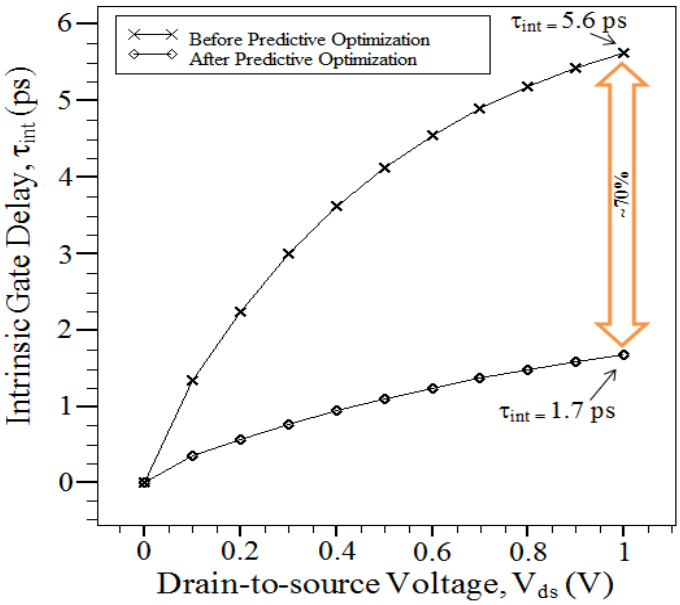

Fig. 9. Overlay plot of the τ_{int} –V_{ds} curve before and after predictive optimization in linear mode

The intrinsic gate delay of the device is extremely small measured at 1.7 psec, implying the optimized device requires lesser time to generate an output for a given input. Thus, it can be concluded that the proposed predictive optimization method using a hybrid MRA-GA model is capable of minimizing the intrinsic gate delay of the device by predicting the optimum magnitude of Ge mole fraction, high-*k* material thickness, source/drain doping concentration and metal work-function. However, the optimization results can be further improved by considering more geometrical and process parameters. The proposed approach could also be applied to other semiconductor devices and engineering problems.

4. Conclusions

In summary, a hybrid model of Multiple Regression Analysis (MRA) and Genetic Algorithm (GA) are utilized as a predictive optimization method to minimize the intrinsic gate delay (τ_{int}) of the n-type JLDGST. The initial approach is to derive a mathematical relationship (objective function) between the dependent variable (τ_{int}) and the independent variables (Ge mole fraction, $T_{high\text{-}k}$, N_{sd} and WF) by using the MRA. In addition, MRA results shows that metal workfunction is the most

significant design parameter contributing the considerable variance on the intrinsic gate delay. After deriving the objective function, the GA is employed by fitting the objective function within the preset upper and lower boundaries called the fitness function (f_i). Throughout the iterative process of selection, crossover and mutation, the most optimum fitness magnitude (11.26682) is identified after 504 cycles of generation. As a result, a hybrid MRA-GA model has successfully reduced the intrinsic gate delay by ~70% in which the optimum Ge mole fraction, $T_{high\text{-}k}$, N_{sd} and WF are predicted to be 0.3 (30%), 3 nm, $2.96x10^{13}$ cm^{-3} and 4.6 eV respectively. Thus, it is concluded that a hybrid MRA-GA model can be one of the practical approaches for reducing the τ_{int} of the device as well as predicting the optimum magnitude of the design parameters. In future work, more design parameters could be considered using the proposed predictive approach for better optimization solutions.

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