Journal of Advanced Research in Applied Sciences and Engineering Technology

Journal homepage:
https://semarakilmu.com.my/journals/index.php/applied_sciences_eng_tech/index
ISSN: 2462-1943

Review of Low Dark Current of Lateral PIN SOI Photodiode for Energy Harvesting Application

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ABSTRACT

The photodetectors family plays an important role in many applications, including for energy harvesting. Extensive research and ongoing development of photodetectors have enriched their functionality and increased their performance. Combining SOI technology with Lateral PIN diode structure, they provide high isolation, low leakage current, and high speed, making them ideal for low light levels and noise-sensitive applications. Although Lateral Silicon-On-Insulator (SOI) PIN diodes have unique characteristics that can be useful in various applications, especially in RF applications, their fabrication and modelling are quite complicated. Meanwhile, a diode with poorly passivated surfaces may have many surface trap centres that contribute to additional dark currents by increasing the recombination of electron-hole pairs. The innovation continues and alters the concept to lessen dark current as of this research. We selectively review the research of SOI-based Lateral PIN photodiode from the point of view of principle and operating performance to obtain optimal dark current values. Silicon photodiodes with a conventional PIN structure are discussed.

Keywords:
SOI photodiode; Lateral PIN; Low dark current; Energy harvesting

1. Introduction

Harvesting energy from the sun and other light sources is appealing since these forms are numerous and have high energy densities when compared to other types of energy found in the environment [1,2]. An energy harvesting device is an innovative solution for powering microelectronic devices in the absence of traditional energy sources by transforming mechanical energy into electrical energy [3]. In the context of energy harvesting applications, photodiodes play a crucial role in capturing and converting light energy into electrical power Operating in photovoltaic mode, photodiodes efficiently generate a photocurrent when exposed to light, making them an ideal

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https://doi.org/10.37934/araset.60.2.4960

component for solar energy harvesting systems. Their ability to harness the abundant and concentrated energy from sunlight and light sources enables sustainable and clean power solutions [4]. Photodiode-based energy harvesting finds diverse applications, from powering low-power devices and wearable electronics to providing energy for autonomous sensors and wireless communication nodes, particularly in areas with limited access to conventional energy sources. This combination of abundant light energy and the efficiency of photodiodes makes the process of harvesting energy from the sun and light sources highly attractive and environmentally beneficial [5].

Typically, photodiodes as semiconductor photodetectors emit a photocurrent after converting incoming photons into free charge carriers. In various fields, such as optical communications, image acquisition, optical spectrometry, and others, the photodetector is an important tool [6-12]. The applications of photodetectors go beyond information technology and include interdisciplinary fields of study such as high-energy physics and optical biological sensors [13,14]. Silicon photodetectors are extensively researched and used due to the low cost of the material [15]. In addition, silicon photodetectors are of great interest and challenge in integrating such receivers for short-range optical communications. Moreover, due to the maturity of the CMOS fabrication process, it is a clear advantage to integrate Si photodetectors into monolithic circuits [15-18].

PN junctions are widely used as optical devices because the electric field in the depletion layer formed between the two regions (P and N) leads to the separation of electron-hole pairs and the increase of the reverse current of the diode. Moreover, the larger the depletion layer, the more light is absorbed; on the other hand, a smaller depletion layer is required to generate a higher electric field [19].

Consequently, the size of the depletion layer must balance sensitivity and response time, as it must be both large enough to absorb the largest number of photons and small enough to shorten the transit time of the generated charge carriers [20,21]. The PIN photodiode is a specific example of a PN junction photodiode and one of the most commonly used photodetectors because the thickness of the depletion region can be adjusted to optimise the quantum efficiency and frequency response. Since this shortens the carrier transit time and decreases the diode capacitance, these photodiodes are often operated with moderate reverse bias voltages [20]. The processes that occur in the intrinsic region are of critical importance because they can change the properties of the depletion layer and, consequently, the collected photogenerated charge carriers. For example, changing the additional gate bias can alter the concentration of carriers in the intrinsic region, which can affect the number of electron-hole pairs collected [19].

The exceptionally low dark current in our device makes it attractive for photodiode applications since a low dark current in a photodetector helps to improve the signal-to-noise ratio [22]. Since the diameter of the light spot is much larger than the size of the device, the light beams illuminating the surface of the device are assumed to be perfectly uniform in the experiment [23].

In this context, due to the particular advantages such as low leakage current, reduced parasitic capacitance, radiation hardness, and variable back-gate tuning, silicon-on-insulator (SOI) technology provides a flexible platform for advanced silicon photonics [24-26]. The use of photodiodes built into SOI wafers can be a successful workaround to this shortcoming [27] such as UV sensors used for sterilization purposes, e.g., COVID-19 disinfection [28]. For systems with low power consumption, RF, high speed, and or radiation hardness, SOI components are attractive. The SOI platform is a good choice for developing low-power imaging systems, high-speed photoelectric interconnects, radiation-hard pixels in aerospace research, and next-generation high-speed systems because it combines the above electrical and optical advantages [29-31]. The buried oxide in these photodiodes promotes the isolation of charge carriers generated in the substrate, making the lateral PIN SOI

photodiode suitable for applications requiring low dark current, high quantum efficiency and sensitivity, and fast response [32,33].

The photodiode can simultaneously achieve high quantum efficiency in the short wavelength region and low quantum efficiency in the long wavelength region by choosing a suitable thickness for the device layer. One of the most important factors that can be used to evaluate doping and crystalline integrity is the minority lifetime. It is inversely related to the dark current. Longer minority carrier lifetimes are possible for high resistivity, high-quality silicon wafers, which is beneficial for lowering dark current [34]. An investigation and analysis of recent developments in SOI photodiode that have led to dark current reduction is presented in this paper.

2. Lateral PIN Photodiode on Silicon-On-Insulator (SOI)

Lateral SOI PIN photodiodes are more advanced than conventional PIN photodiodes due to their superior performance in terms of high speed, high sensitivity, low noise, and low dark current. One of the main advantages of lateral SOI PIN photodiodes over traditional PIN photodiodes is their ability to combine the advantages of SOI (Silicon on Insulator) technology with PIN diode structure. The SOI technology enables the fabrication of high-performance devices with excellent isolation, low leakage current, and high speed [35], while the PIN diode structure offers high sensitivity, low noise, and low dark current, which is critical for applications where noise must be kept to a minimum or for applications where low light levels must be detected [36].

2.1 Device Structure

The PIN diode is a particular instance of the PN junction photodiode and one of the most common photodetectors [37] since the intrinsic depletion zone may be modified to optimise the quantum efficiency and frequency responsiveness. As shown in Figure 1, the PIN diode is made up of a PN junction separated by an intrinsic (I) region and an intrinsic length region (L_i).

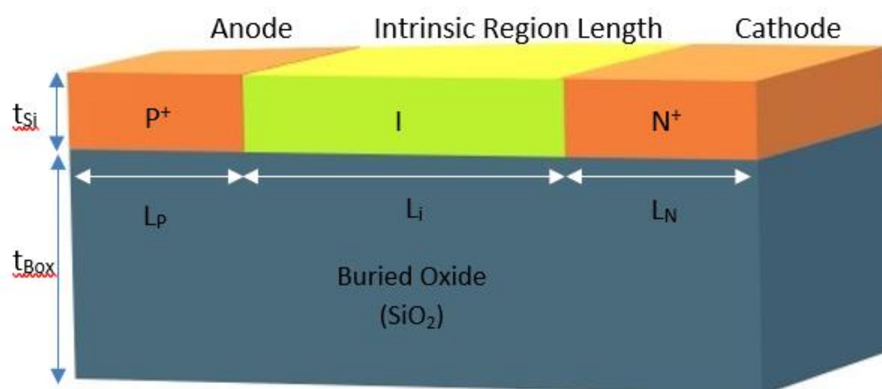

Fig. 1. Lateral PIN SOI photodiode structure [38]

The intrinsic region could be a low-doping P-type or N-type zone depending on practice. The depth to which the substance is pierced determines the amount of light that is absorbed. Lateral PIN SOI photodiodes constructed in thin silicon sheets are good choices for short wavelength absorption [39]. UV and blue light penetration depths in silicon, for example, are roughly 100 nm and 500 nm, respectively. The width of the intrinsic region of PIN photodiodes can be adjusted to improve quantum efficiency and responsiveness [40]. Furthermore, placing the silicon film on top of a buried oxide layer enhances separation between the photogenerated carriers and the substrate, reducing

the device's dark current, boosting efficiency, and low capacitance, while also increasing frequency response [41].

2.2 Latest Experiment of Lateral PIN Diode

In 2007, Aryan *et al*., [42] proposed a structure that combines the advantages of the SOI material and the lateral PIN photodiode in a CMOS-compatible structure, as shown in Figure 2.

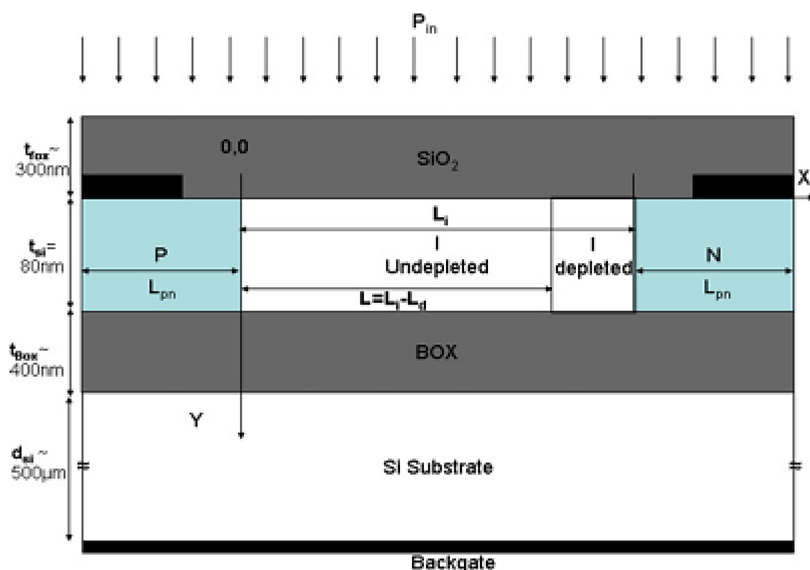

Fig. 2. The schematic cross-sectional view [42]

The experiment performed measurements of the dark current and optical sensitivity of thin-film SOI diodes from the UV to the near IR region (200-850 nm) at V_d = -3 V for different lengths of the intrinsic zone (L_i). From the measurement of developed modelling, QE demonstrated in more than 60% (90% with an ARC), a very low value of dark currents in SOI, which can provide, see Figure 3, a high ratio of more than 106 between illuminated to dark currents with the low input power for Blue DVD (a few µW of incident optical power and a typical photodiode area of 50 µm x 50 µm), for example.

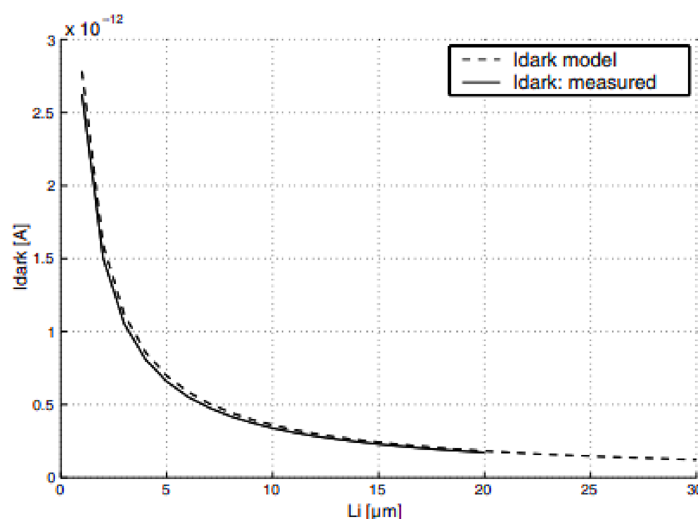

Fig. 3. Measured dark current of a lateral SOI PIN photodiode by experiment [42]

In 2014, Novo *et al.*, [43] presented the influence of back-gate bias on the performance of lateral SOI PIN photodiodes at high temperatures between 300K and 500K. A schematic cross-section of the device studied is shown in Figure 4, along with the thicknesses and intrinsic lengths, which are summarised in Table 1 along with the doping concentrations and total area.

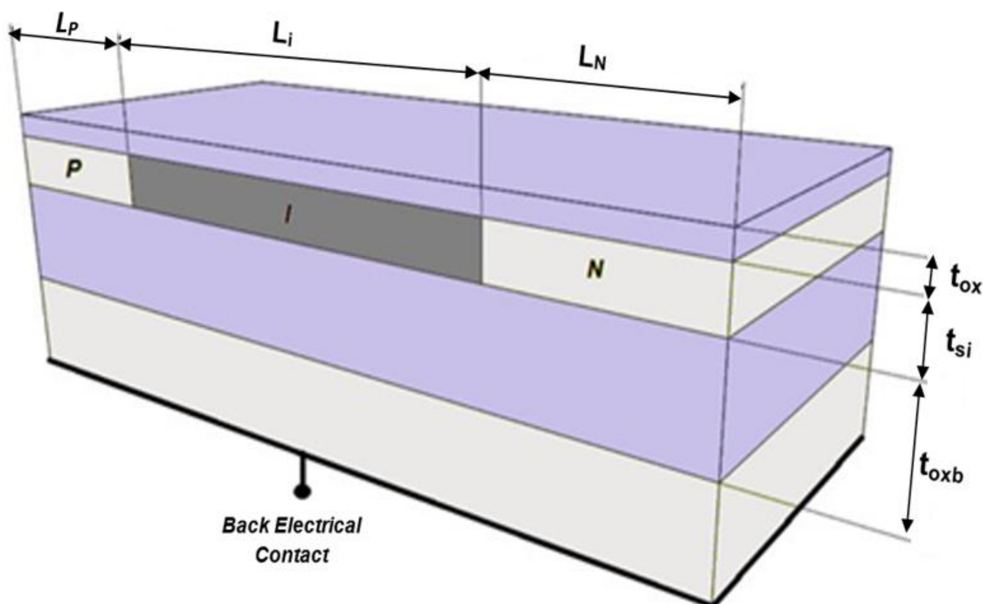

Fig. 4. The schematic cross-sectional view of one finger of a lateral SOI PIN photodiode on SOI by experiment [43]

Table 1
Lateral SOI PIN technological parameters and dimensions

Parameter	Values
Silicon film thickness, tsi	80 nm
Buried oxide thickness, t_{ox}	390 nm
Passivation oxide thickness, t_{ox}	280 nm
Intrinsic region doping concentration, N_1	1 x 10^{15} c
P region doping concentration, N_A	1 x 10^{20} c
N region doping concentration, N_D	4 x 10^{20} c
Total width (L_I = 8 µm)	14.5 mm
Total width (L_I = 9 µm)	55.0 mm
Total area (L_I = 8 µm)	0.25 mm^2
Total area (L_I = 9 µm)	1 mm^2
N and P length (L_P, L_N)	9 µm

In some applications, photodiodes are exposed to high temperatures that affect their performance as well as V_{BG} [43]. For example, the IDR in accumulation mode (V_{BG} = -20 V) can be almost five times higher at a temperature of 480 K than at V_{BG} = 0 V. The decrease in dark current is mainly responsible for the increase in IDR ratio in accumulation mode (V_{BG} = -20 V). The overall quantum efficiency of the device increases with temperature and can reach 86% at T = 500 K in depletion mode (V_{BG} = -2 V). Figure 5(a) and Figure 5(b) show that the back-gate bias affects the photocurrent and dark current for three different silicon layer thicknesses [47], with the I_{DARK} decreasing and the photogenerated current decreasing for very thin devices. As shown in Figure 3, the dark current of both detectors increases with increasing temperature [43-46].

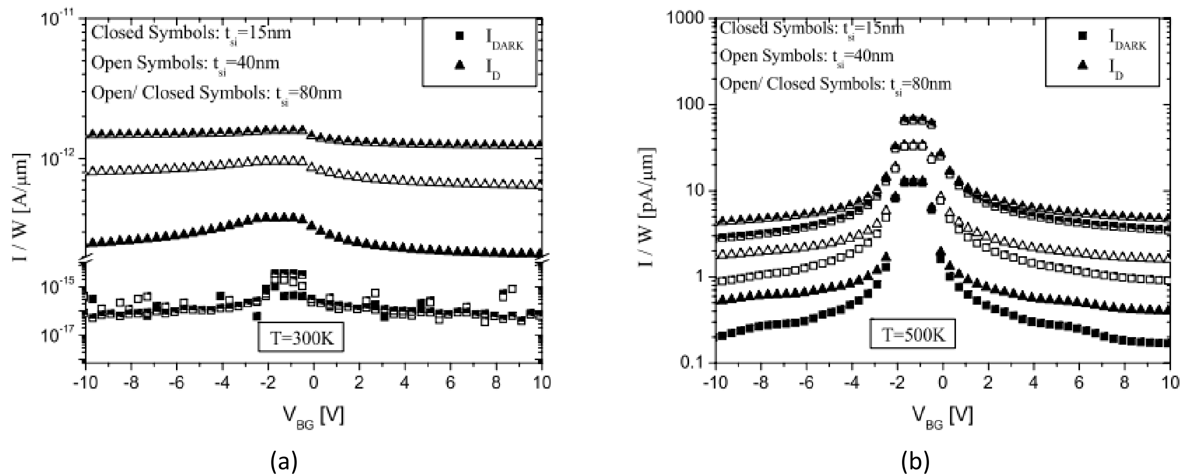

Fig. 5. Photocurrent and dark current as a function of V_{BG} for different silicon thicknesses for λ = 400 nm at (a) T = 300 K (b) T = 500 K. Adapted from [43]

In 2020, the conventional PIN diode used ion implantation to form the doped regions. To avoid damage to the ultra-thin Si layer and the associated high dark current, Liu *et al.*, [48] demonstrated a lateral PIN diode with field-induced doping.

As shown in Figure 6, the device is based on an SOI substrate with undoped 100 nm top silicon and 145 nm buried oxide. The fabrication process includes photolithography, wet etching, thermal evaporation, gate electrode formation, and low temperature annealing to improve Schottky contacts on SOI substrate.

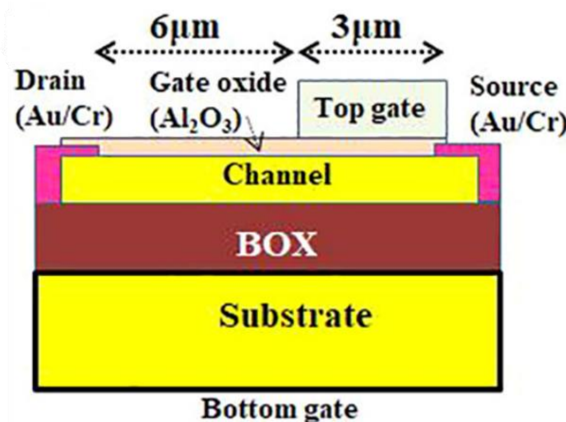

Fig. 6. Schematic view of the device [48]

Since the diameter of the light spot is much larger than the size of the device, the light rays projected onto the surface of the device are completely uniform [49]. The output characteristics of the fabricated device are shown in Figure 7 as a function of optical power density, which ranges from 10 to 1000 W/cm^2. As the optical power density increases, the reverse current also increases dramatically. The open-circuit voltage (V_D at I_D = 0) moves toward positive V_D values in proportion to the optical power density, similar to a typical photodiode. Even 10 W/cm^2 weak illumination intensity can result in observable photocurrents nearly an order of magnitude above the dark current. The low dark current density of 2.5 nA/cm^2 is due to the undamaged Si layer, which is not subjected to ion implantation or high-temperature annealing [48].

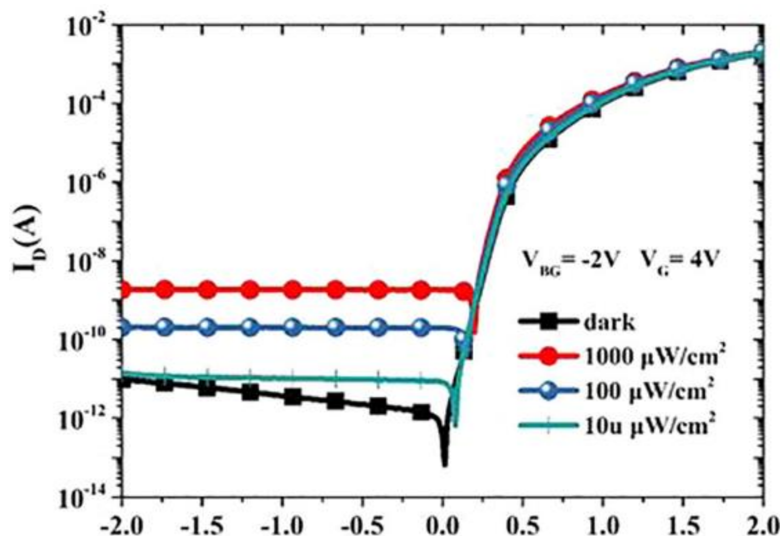

Fig. 7. The I_D-V_D characteristics of the device under λ = 520 nm illumination as a function of intensity in the 10–1000 μW/cm^2 range [48]

Overall, Table 2 lists some significant progress and recent developments in lateral SOI PIN photodiode.

Table 2
Summary of the review dark current in the latest research of Lateral SOI PIN photodiode

Ref.	Method	Variation of different parameters	Dark Current
Aryan *et al*., 2007 (Characterization of quantum efficiency, effective lifetime, and mobility in thin film ungated SOI lateral PIN photodiodes)	Analytical Model of lateral SOI PIN photodiode in CMOS-compatible structure	different lengths of the intrinsic zone (L_i)	Lower than pA
Novo *et al*., 2014 (Illuminated to dark ratio improvement in lateral SOI PIN photodiodes at high temperatures)	Simulated by Atlas Software	1. thicknesses and the intrinsic length which are summarized with the doping concentration levels and the total area 2. Operating Temperature	Has its maximum value for V_{BG} = -3V for T = 500K
Liu *et al*., 2020 (photodiode with low dark current built-in silicon-on-insulator using electrostatic doping)	Electrostatic doping (photolithography, wet etching)	I-V characteristics of the fabricated device operated with constant V_{BG} = −2 V for V_G = −4, 0, and 4 V	down to 2.5 nA/cm^2

3. Conclusions

Research on photodetectors with low dark current is presented here. The other component of the device contributes to the dark current at a level that is about four orders of magnitude lower. The photocurrent and dark current present lower values as the silicon film thickness is decreased. The rise of temperature increases the dark current (I_{DARK}) by several orders of magnitude, as a result of increased thermal generation of electrons [50]. The electrostatically induced diode has a low dark current, excellent optical response, linearity, enhanced near-UV response, and can be switched between photodiode mode and resistor mode, potentially for selective access in a photodetector

array. More experiments are needed with simpler and more effective methods to get a lower dark current value. One effective approach to reducing dark current involves optimizing the thickness of the thin films. Thin film thickness optimization offers several advantages. It allows researchers to explore a fundamental aspect of device physics – how carrier diffusion and recombination processes are affected by film thickness. Incorporating thin film thickness optimization as an experimental approach can contribute to the ongoing efforts to reduce dark current in photodetectors. Its simplicity and potential for significant impact make it a valuable method for us seeking practical ways to enhance photodetector performance.

Acknowledgment
This research was supported by Universiti Tun Hussein Onn Malaysia (UTHM) through Tier1 (vot Q486) and the Ministry of Higher Education (MOHE) through the Fundamental Research Grant Scheme (FRGS) FRGS/1/2020/TK0/UTHM/02/46.

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