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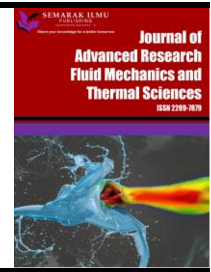

Investigating Thermal Performance of Substrate Board through Forced Convection and Machine Learning

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ABSTRACT

In this study, the thermal performance of substrate board exposed to forced convection with different heat source configurations was investigated. Seven asymmetric integrated circuit chips (heat sources) positioned at various points on the substrate board were cooled through steady-state experiments using laminar forced convection heat transfer mode. The objective was to determine the optimal layout of the seven integrated circuit chips on the board for lowering the maximum temperature. The optimal configuration was determined experimentally and was further validated by employing a machine-learning optimization strategy. Various correlations have been proposed to investigate the effect of the substrate board arrangement on the integrated circuit (IC) Chip temperature and heat transfer coefficient. These findings imply that the size and configuration of the substrate board, input heat flux, and placement of the IC chips have a significant impact on their temperature. Because the heat is discretely placed in this scenario, the temperature of the integrated circuit (IC) chips is the lowest for higher values of the non-dimensional parameter λ. This aids in efficiently reducing the temperature of chips through cooling. Another important factor in the cooling of IC chips is air velocity. The maximum temperature reduction is 14.02% at an air velocity of 3.5 m/s.

1. Introduction

The rapid expansion of the electronics industry and the ongoing struggle to make the most use of the available space have resulted in smaller integrated circuit chips and electronic components. The performance and reliability of integrated circuits are affected by the shrinking of their sizes, which increases volumetric heat generation in the chips. The difficulty lies in extending the operational cycle of the IC chip by using various cooling methods. Air-cooling is the most accessible and economical option for this purpose. To remove the maximum amount of heat from IC chips, most electronic components are accompanied by a fan and undergo forced convection cooling. In addition, the placement of IC chips on the substrate board plays an important role in the cooling of the IC chips.

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Dhumal *et al.,* [1] studied the advances in electronics and new application areas and presented the potential for novel materials to handle thermal management issues. Currently, electronics face substantial thermal management difficulties, but innovative materials are emerging to address them. The scale of power dissipation and semiconductors were at different locations, necessitating the development of new cooling methods to cut costs without sacrificing cooling efficiency. Durgam *et al.,* [2] conducted transient numerical calculations on four identical protrusion heat sources operating in the forced and natural convection heat transfer modes. They investigated the impact of heat transfer on the heat source spacing, heat transfer modes, and board thickness for both horizontal and vertical board orientations. Doğan *et al.,* [3] experimentally investigated the heat transfer properties of rectangular flush-mounted heat sources in mixed-convection heat transfer mode. They noted that the heat sources that released the most heat must be positioned at the entry or exit of the channel. The cooling of heat sources installed on a vertical printed circuit board (PCB) was investigated experimentally and numerically by Mebarek-Oudina *et al.,* [4]. They established a relationship between the airflow, substrate temperature, heat-source configuration, and Nusselt number of heat sources.

Che *et al.,* [5] numerically analyzed three flush-mounted heat sources for cooling using the laminar forced convection heat transfer mode. They suggested that the superposition principle with an influence coefficient could be used to forecast the temperature of heat sources. Hamouche and Bessaïh [6] numerically examined the impact of the height and separation between the two heat sources under laminar mixed convection heat transfer mode using air. The heat transfer of the IC chips was improved by 5 Q_supp = V_S I ≤ Re≤ 50, and Pr = 0.7. Lintang [7] used Fluent to perform numerical simulations on a plastic lead -chip carrier (PLCC) installed on a printed circuit board (PCB). The temperature, Nusselt number, and thermal resistance were tested by altering the heat flow, air velocity, and distance between PLCC. The thermal performance of the PLCC improved with an increase in air velocity. Gibanov and Sheremet [8] reviewed in depth the heat transport from IC chips through natural convection. Because natural convection can only dissipate heat up to 1000 W/m^2, higher heat dissipation methods, such as heat sinks and liquid immersion cooling, can be used. Pirasaci and Sivrioglu [9] investigated experimentally, using varied heights and widths for various Reynolds numbers and adjusted Grashof numbers, the impact of mixed convection heat transfer on 32 projecting heat sources. The findings revealed that buoyancy-induced flow increases the rate of heat dissipation at lower Reynolds numbers. He *et al.,* [10] examined the properties of an air-powered flush-mounted heat source for heat transmission both computationally and empirically. They concluded that high-emissivity heat sources were optimal. Hotta and Venkateshan [11] conducted steady-state tests for five asymmetric heat sources installed on a vertically oriented substrate board, using both natural and mixed convection heat transfer modes. The heat transfer types for the respective heat dissipation rates were compared. The authors concluded that mixed convection is a better method for cooling the heat sources. In connection with this, numerical analysis is conducted by Karvinkoppa and Hotta [12].

Ajmera and Mathur [13] conducted studies on three flush-mounted heat sources using mixed and natural convection heat transfer modes. The heat sources with the highest and lowest temperatures were positioned at the channel entrance and exit, respectively. Mathew and Hotta [14] utilized ANSYS-Icepak, an ideal arrangement of seven asymmetric integrated circuit chips installed on a Switch Mode Power Supply (SMPS) board under mixed convection heat transfer mode was numerically examined. It was determined that the lowest edge of the substrate board should house the IC chips with the highest temperature. Pour and Esmaeilzadeh [15] investigated through experimentation how the electrohydrodynamic (EHD) actuator dissipates heat from cylindrical heat sources that are housed inside ducts. It was discovered that the Reynolds number increased the heat

transfer for the cylindrical heat sources, and the EHD actuator was crucial for cooling IC chips. Bouraoui and Bessaïh [16] conducted numerical simulations for two identical heat sources to investigate the effects of aspect ratio, Rayleigh number, and heat source spacing on the rate of cooling under the natural convection heat transfer mode. They noticed that when the aspect ratio and separation between the heat sources increased, the Rayleigh number also increased. Six heat sources were subjected to numerical simulations using the mixed-convection heat-transfer method proposed by Chaurasia *et al.,* [17]. By adjusting the air velocity, thermal conductivity, and emissivity of the heat sources, they discovered a significant temperature reduction in the heat sources. Mele and Ruocco [18] conducted numerical and analytical research to determine the best location for heat sources under forced and natural convection heat - transfer modes. The results indicated that the heat sources should be placed at the channel entry for a higher Reynolds number.

Venkatachalapathy and Udayakumar [19] investigated 20 protrude-mounted heat sources operating in the mixed convection heat transfer mode, which were the subject of experimental and numerical investigations. All sources were housed in enclosed enclosures. In comparison with the heat sources positioned at the inner surface, they discovered that the heat source near the entry cooled first and had a greater Nusselt number. Hotta *et al.,* [20,21] used a hybrid optimization approach (ANN+GA) powered by experimental data to conduct an experimental examination of five non-identical heat sources operating in the mixed convection heat transfer mode to identify the ideal placement of the IC chips. They recommended that the heat source be positioned at the lowest point of the substrate board to achieve its maximum temperature. Godi *et al.,* [22] conducted experimental studies to ascertain the local heat transfer coefficient using planar and three-dimensional wall jets across a level surface. They concluded that turbulent jets are crucial in various technical applications, including the cooling of gas- turbine blades, liners, and electronic components. Pérez-Flores *et al.,* [23] conducted temporary mixed convection within a cavity with separate heaters. They investigated the impact of channel aspect ratio, buoyancy, and inclination angle on the heat transfer properties of the heat source. Habib *et al.,* [24] used a uniform and non-uniform supply of heat flux to experimentally examine protrude-mounted heat sources in the natural convection heat transfer mode. In comparison with their uniform distributions, they discovered that a non-uniform heat source distribution produced superior cooling. Mathew and Hotta [25] conducted numerical and experimental studies on various board orientations for seven distinct λ configurations. The aim was to determine the ideal arrangement for the IC chips and substrate board orientation.

Recent research has explored the use of machine- learning algorithms in the thermal management of electronic devices. Dai *et al.,* [26] developed a tool for product designers to evaluate thermal resistance characteristics using neural network models and ensemble learning. Chharia *et al.,* [27] discussed the use of deep learning in electronic thermal management to address the limitations of the traditional numerical techniques. Li *et al.,* [28] used machine learning models to predict the evolution of parameters in power electronics modules and, achieved satisfactory performance in industrial embedded systems. Li *et al.,* [29] applied Bayesian Optimization in 3-D ICs for the intelligent control of microfluidic heatsinks, enhancing dynamic thermal management. These studies collectively demonstrate the potential of machine learning to improve the efficiency and lifespan of electronic devices through effective thermal management.

It is evident that the majority of research on the cooling of integrated circuits (ICs), whether protruding or flush mounted, has been conducted using natural and mixed convection heat transfer modes. Most of the evaluations considered symmetric IC chips with constant heat flux. Surprisingly, few experimental investigations have addressed the vertical or horizontal orientation of substrate boards. A broader area, rarely covered in the literature, was also explored by examining seven integrated circuits. Therefore, the analysis of the seven asymmetric integrated circuit chips supplied

with non-uniform heat fluxes under the laminar forced convection heat transfer mode is the focus of this study. The goal was to find the best configuration for IC chips on a substrate to reduce their temperature using experimental forced convection and machine learning.

Dhumal *et al.,* [30] investigates the effect of different fin configurations on the thermal performance of radiators, finding that higher fin density (10 FPI) improves thermal performance.

WafirulHadi *et al.,* [31] investigates thermal properties of PCM during the discharge process and cycle tests play important role of increasing natural convection and heat conduction in the PCM structure, thereby increasing the efficiency of heat dissipation and reducing the risk of failure in a passive thermal management system using PCM. The utilization of cooling system of PCM and heat pipes can increase the effectiveness of thermal management n battery of electric vehicle.

2. Materials and Methodology

A schematic layout of the low-speed horizontal wind tunnel setup used in this study is shown in Figure 1. The effuser (inlet duct), test section, axial flow fan, diffuser, and motor with a speed control unit are many components of a wind tunnel. To directly direct and align the airflow to the test portion, the Effuser was composed of a honeycomb part. It has a 9:1 contraction area ratio and is aerodynamically shaped. The effuser's inlet measured 90 cm × 90 cm and was curved to measure 30 cm × 30 cm. The axial and lateral turbulences were reduced using a honeycomb and screens, and a smooth airflow to the test section was produced. To prevent turbulence and preserve a smooth airflow, a wire mesh was added. With the employment of a flange, the diffuser and input duct (effuser) were positioned between the central areas of the test section. It was fixed, making it easier to fix and view the models with transparent windows on either side. The axial flow fan was connected to a diffuser unit located downstream of a wind tunnel. At the end of the test section, the diffuser measured a 30 cm × 30 cm square, and at the fan-driven end, it expanded to 120 cm in diameter. The test section is fastened and flanged. The fan unit was grounded to reduce vibrations and was of an independent standalone variety. The diffuser was fastened to a circular shell that contained the device. There are two consoles in the wind tunnel: one for airspeed control (AC motor controller) and the other for the velocity head indicator.

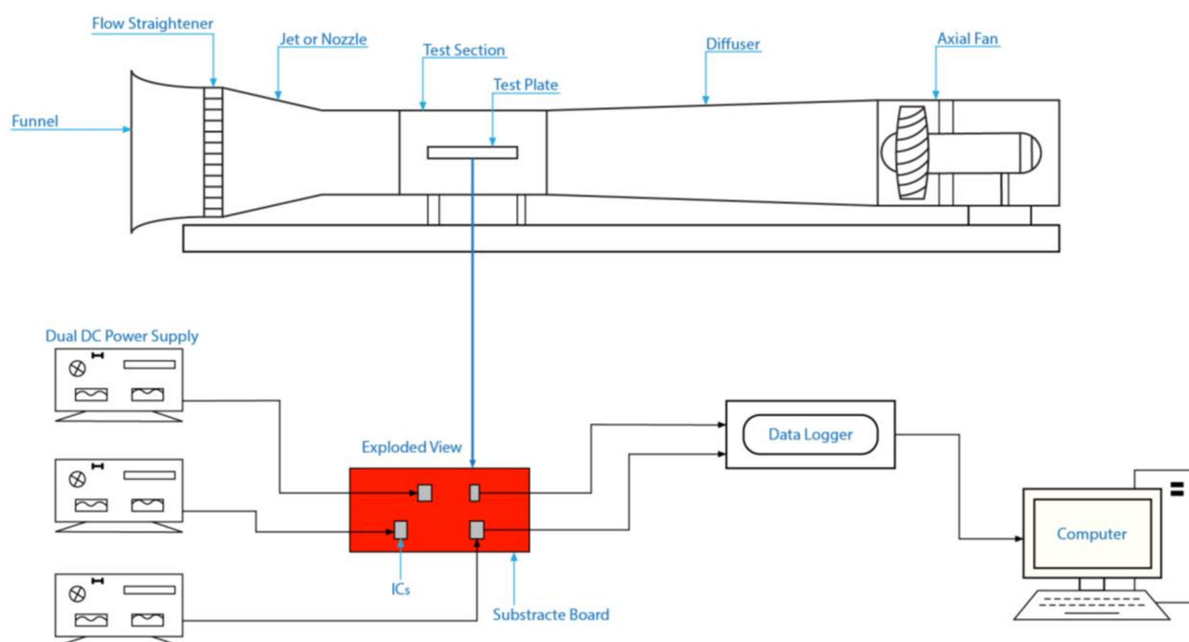

Fig. 1. Schematic layout of the experimental set-up

Figure 2 shows the layout of the aluminum blocks that were modeled after the real IC chips. 80% nickel and 20% chromium, or 80/20 coil-type Nichrome wires were used in a heater to facilitate the power input to the integrated circuit chips. Each heat source had a recess created on the bottom face of the heater wires, which were then insulated using Teflon tape. The heater and thermocouple wires were positioned in slots on the bottom face of each heat source. These wires were then linked to a dual- output DC power source (MULTISCOPE) with voltage and current ranges of 0–30 V and 0–2 A, respectively.

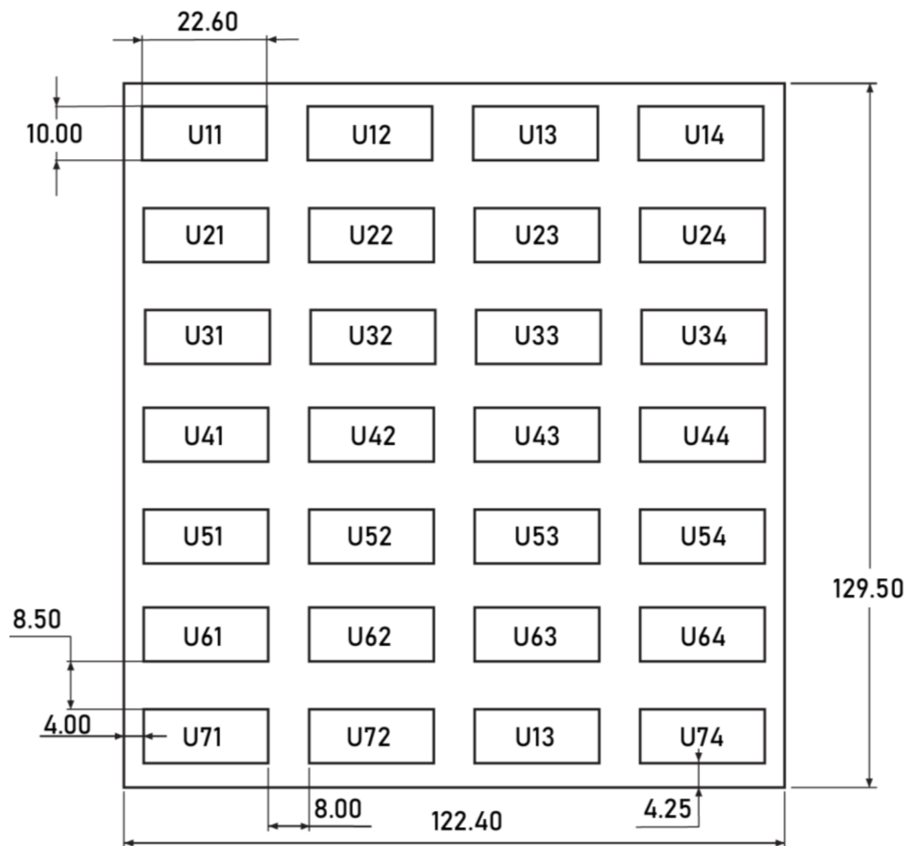

Fig. 2. Layout of the substrate board (All dimensions are in mm)

K-type thermocouples were used to measure the temperature of the integrated circuit chip. Each thermocouple was calibrated at the ice point and boiling point of water using a standard mercury thermometer; the measurement error was found to be ±0.2°C. Two thermocouples were installed on the substrate board to measure the temperature of the board, and one at the bottom of each integrated circuit chip. An anemometer with hot wire was used to measure the air velocity in the test section. The substrate board was split into seven rows and four columns (7 × 4) to position the seven asymmetric IC chips. Figure 2 shows the dimensions of the substrate board at 28 locations.

The seven IC chips on the board can be placed in 28 different ways (28P7), using 28 available locations or slots. A geometric distance parameter, which is a non-dimensional parameter λ, was used to identify each arrangement. With the installation of the thermocouple and heater wires, each IC chip was placed on the substrate pieces (28 substrate pieces from 28 slots on the board). The substrate board had seven spaces that could hold the seven IC chips, with the remaining twenty-one spaces occupied by the leftover substrate pieces.

The steps involved in carrying out steady-state experiments using the laminar forced convection heat transfer mode are outlined below.

First, uniform air velocity was delivered to the test portion (substrate board with IC chips)

(through the axial flow unit of the wind tunnel). Turning on the DC power source and modifying the necessary voltage and current will set the appropriate heat input to the IC chips (the heat flux from Table 1 is transformed into heat input). Eq. (1) was used to determine the required heat input.

$$Q_{supp=V_s\,I} \tag{1}$$

Table 1
Specifications of the different parts that are fixed to the substrate board

Components	Dimensions (l_c x w_c x t_c), cm)	Heat Flux (q), W/cm^2
U1	1.01 X 1 X 0.77	0.7
U2	0.93 X 1 X 0.78	0.6
U3	0.8 X 1 X 0.78	0.9
U4	1.82 X 1 X 1.55	0.3
U5	1.23 X 1 X 1.26	0.4
U6	0.41 X 1 X 0.82	0.4
U7	0.83 X 1 X 0.77	0.3
Substrate board	129.5 X 122.40 X 8.85	NA

After the temperature logger reached a steady state (a temperature change of no more than ± 0.1 C), scanning of the temperature logger was started via the Serial Communication Port (SCP), and the temperature data of the IC chips from each thermocouple were recorded on the computer. According to the manufacturer's catalog, the thermocouple has a time constant of 0.39 s and records temperature at a frequency of one second. In addition, the voltage and current of the DC power source are captured. Next, the excess temperature of each IC chip, that is, the difference in temperature between the chip and the surrounding air, is computed using Eq. (2).

$$T_{excess} = T_{hs} - T_{\infty} \tag{2}$$

Eq. (3) and Eq. (4) were used to compute the radiation heat loss from the IC chips and conduction heat loss to the substrate board, respectively. Given that the chip surfaces were flat and exposed to ambient light, the form factor (F) was assumed to be 1, and the surface emissivity (ε) of the IC chips was 0.08 (as stated by Hotta *et al.,* [21]). Consequently, the energy released from the IC chip surface did not fall on any other surfaces.

$$Q_{cond} = \frac{K_{sub}A(T_{hs}-T_{\infty})}{t_{sub}} \tag{3}$$

$$Q_{rad} = F\varepsilon\sigma(T_{hs}^4 - T_{\infty}^4) \tag{4}$$

$$Q_{conv} = Q_{supp} - Q_{cond} - Q_{rad} \tag{5}$$

$$h_{conv} = \frac{Q_{conv}}{A(T_{hs}-T_{\infty})} \tag{6}$$

Eq. (5) provides the energy balance formulation used to compute the convection rate from the surface of the IC chips. Using Eq. (6), the convectional contribution that causes the IC chips to cool is computed.

The formula provided in Eq. (7) was used to calculate the thermal resistance, which is a crucial characteristic for the thermal management of IC chips. The thermal resistance is inversely

proportional to the amount of heat supplied. Consequently, as the heat input increases, the thermal resistance decreases. As shown in Table 1, various integrated circuits (ICs) were subjected to different heat fluxes.

$$R_{th}=\frac{T_{hs}-T_{substrate}}{Q_{supp}} \tag{7}$$

Figure 3 illustrates the variation in the thermal resistance for each IC chip at different velocities. As previously mentioned, varying heat fluxes are assigned to different ICs, which accounts for the disparity in the thermal resistances among the ICs. Additionally, it was observed that, as the velocity increased, the thermal resistance of the ICs decreased. This phenomenon occurs because the heat transfer rate increases with an increase in velocity.

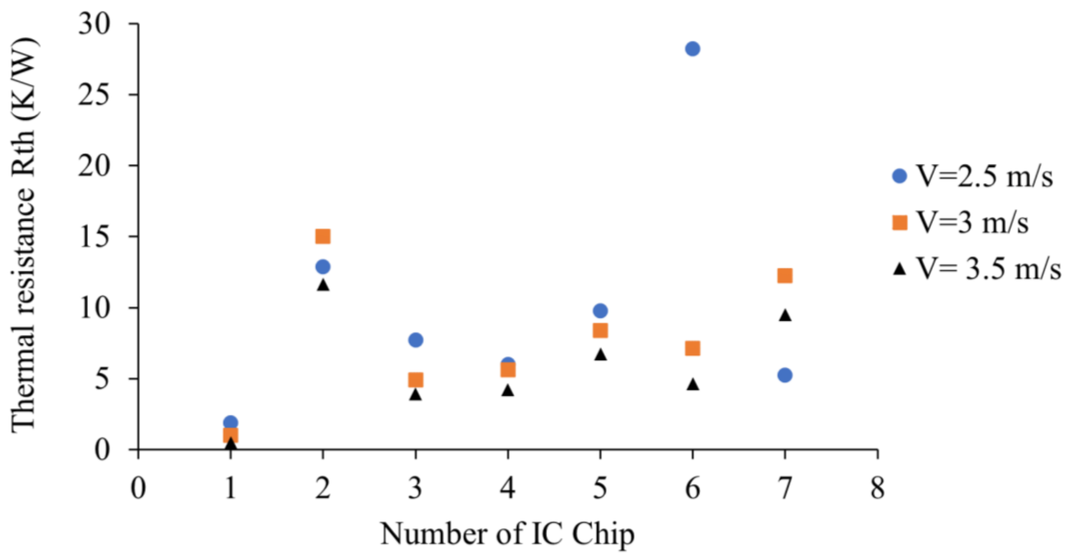

Fig. 3. Thermal resistance variation of all the IC chips for λ= 2.17935 at different velocities

2.1 Non-dimensional Geometrics Distance Parameter (λ)

Seven non-identical rectangular heat sources were arranged in 1184040 distinct ways on a printed circuit board (PCB). Each configuration was distinguished by a distinct λ, which ranged from 0.1690 to 2.1790. Writing the MATLAB code yielded various setups and their respective λ values, as stated by Mathew and Hotta (2018). Size and location affect the nondimensional geometric distance parameter. Eq. (8) was used to calculate λ.

$$\lambda = \frac{\Sigma_{i=1}^{7} d_i^2}{l^2 + Y_c^2} \tag{8}$$

The subscript 'i' is the IC chip number. In equation $\sum_{i=1}^{7} d_i^2$ is Σ [$(X_i - X_c)^2 + (Y_i - Y_c)^2$], where ($X_i$, Y_i) are the centroids of the i-th heat source measured from the x and y-axis of the substrate board, respectively, and (X_c, Y_c) denotes the centroid of the configuration.

2.2 Uncertainty Analysis

The primary and derived quantities of the experiment were subjected to uncertainty analysis. The uncertainties of the primary quantities were determined by calibrating the equipment used to

measure the basic quantities using an accurate standard instrument. A digital multimeter was used to calibrate the voltage and current readings of the DC power supply, and a mercury thermometer was used to calibrate the thermocouples. The uncertainties associated with the measurement of the derived quantities were computed based on the uncertainties of the primary quantities and error propagation formula in Eq. (9). Table 2 lists the uncertainty values for the primary and derived quantities used in the experiment.

$$\nabla\alpha = \pm\sqrt{\sum_{i=1}^{n}(\frac{\partial\sigma}{\partial m_i} \times m_i)^2} \quad (9)$$

In this case, the primary (measured) values are denoted by m and σ, respectively, and the errors associated with the primary and derived quantities are represented by Δm and ∇Q

$$\nabla Q = \sqrt{(\frac{\partial Q}{\partial V} \times \partial V)^\wedge 2 + (\frac{\partial Q}{\partial I} \times \partial I)^\wedge 2} \quad (10)$$

Table 2
Uncertainty involved in the physical quantities

Sr. No.	Measured quantity	Uncertainty value	Unit
1	Current (measured)	±0.002 (full scale)	A
2	Voltage (measured)	± 0.05 (full scale)	V
3	Temperature (measured)	±0.2 (full scale)	°C
4	Velocity (measured)	± 0.1 (full scale)	m/s
5	Power input (derived)	±0.0583	W
6	Heat transfer coefficient (derived)	±0.0011	W/m^2K
7	Thermal resistance (derived)	±2.51	°C/W

3. Results and Discussion

A non-dimensional geometric distance parameter, λ, was assigned to each configuration (the arrangement of the IC chips), and it was discovered that this value strongly depends on the size of the IC chips, where they are located on the SMPS board and input heat flux values. The expression for λ can be obtained using Eq. (8).

The current study aims to identify an ideal design for IC chips to limit their maximum temperature. From the entire range of λ values, thirty-two distinct configurations were chosen at random for the experimental analysis such that they fell between the lower extreme (0.1690) and upper extreme (2.1790) λ values, with the remaining λ values being distributed evenly between the two. Steady-state experiments were performed using 40 distinct setups (Table 3).

Table 3
Various configurations of the IC chips explored for the experiment

Non-dimensional geometrical parameter λ	Configuration U1-U2-U3-U4-U5-U6-U7	Non-dimensional geometrical parameter λ	Configuration U1-U2-U3-U4-U5-U6-U7
0.169091	16-26-15-27-17-14-25	1.19981	11-12-13-37-35-17-42
0.220627	17-35-16-27-25-26-36	1.25134	11-12-13-17-31-32-37
0.272096	11-12-13-22-14-24-23	1.30288	11-12-13-14-33-44-43
0.323652	11-12-13-21-23-31-22	1.35442	11-12-13-26-21-17-47
0.375236	11-12-13-21-23-31-22	1.40595	11-12-15-14-47-31-46
0.42677	11-12-13-24-16-23-14	1.45749	11-12-14-41-26-25-47
0.478303	11-12-13-32-23-25-22	1.50903	11-12-13-41-46-15-45
0.529843	11-12-14-22-23-15-32	1.56056	11-12-26-42-41-15-16
0.581368	11-12-13-27-23-15-24	1.61211	11-12-16-41-43-14-46
0.632915	11-12-13-33-25-14-31	1.66363	11-12-31-43-22-17-47
0.68446	11-12-13-36-25-14-35	1.71516	11-12-31-41-42-26-47
0.735984	11-12-13-16-26-25-32	1.76676	11-12-27-17-42-41-47
0.787521	11-12-13-31-32-14-15	1.81824	11-12-14-31-41-17-37
0.839052	11-12-14-35-37-33-13	1.86978	11-12-16-41-44-47-27
0.890598	11-12-13-27-16-32-34	1.9214	11-12-17-21-41-15-47
0.942132	11-12-13-15-45-26-32	1.97262	11-12-13-31-41-17-47
0.993668	11-12-14-15-44-13-42	2.02438	11-1217-21-41-16-47
1.04518	11-12-13-46-15-14-43	2.0759	11-17-12-41-42-27-47
1.09674	11-12-13-25-47-17-22	2.12701	12-26-31-11-41-47-17
1.14828	11-12-13-35-42-27-31	2.17935	12-31-46-11-41-17-47

Figure 4 shows the greatest temperature surplus across the seven λ combinations. The average temperature of the configuration (average of seven IC temperatures) is the largest for lower λ and smallest for higher λ, indicating that the thermal interaction between IC chips is stronger for lower λ values. At λ= 2.17935, the average temperature of the configuration is minimal. As λ increased, the thermal interaction decreased because of the evenly dispersed IC chips. The effect of air velocity is also clearly observed; with an increase in velocity, the average temperature of the configuration decreases, and it is minimum for 3.5 m/s.

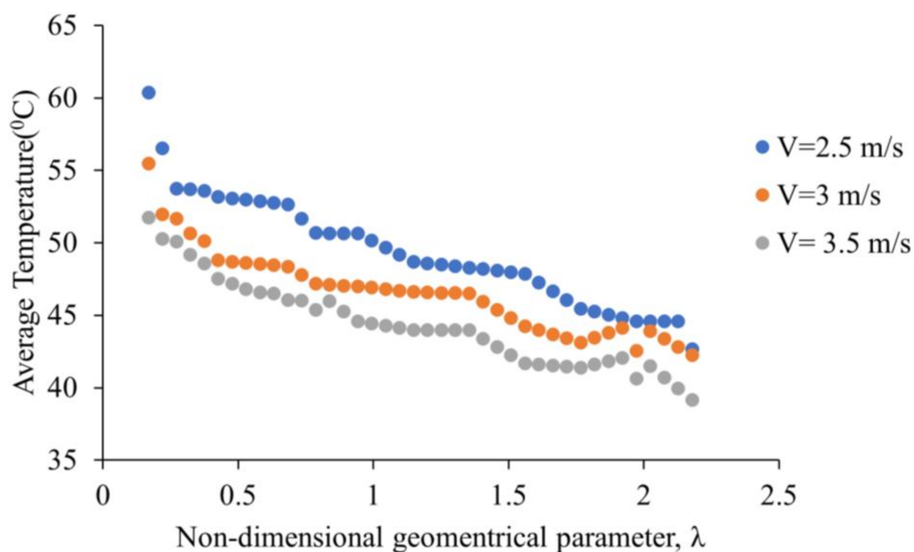

Fig. 4. Variation of average temperature with non-dimensional parameter at λ = 2.17935

Figure 5 shows the variation in the convective heat transfer coefficient with the nondimensional geometric parameter λ. Using the equations provided by Hotta *et al.,* [21], the convective heat transfer coefficient was estimated to assess the cooling performance of integrated circuits. The heat-transfer coefficient increased with λ. At λ = 2.17935, the heat transfer coefficient was higher, indicating a lower maximum temperature for the IC compared with the other designs.

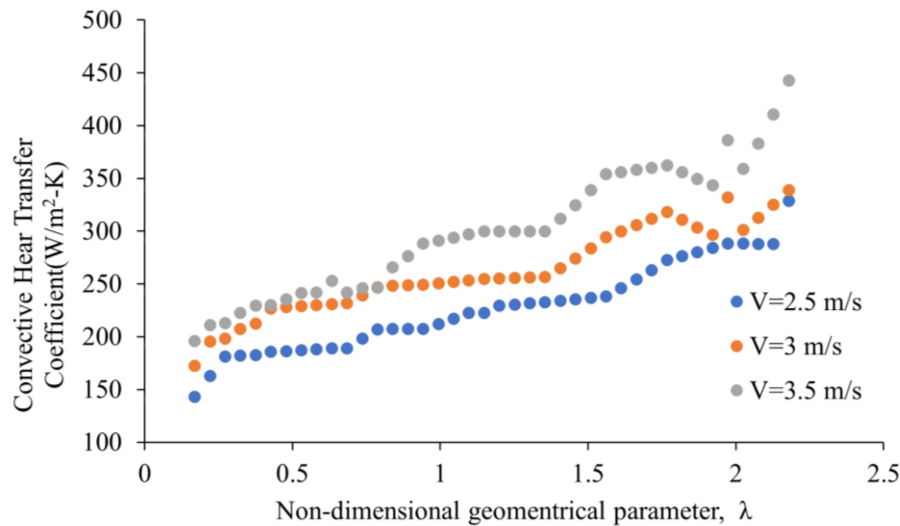

Fig. 5. Variation of convective heat transfer coefficient with non-dimensional geometric parameter, λ

Figure 6 depicts the temperature change in the IC chips installed on a horizontal substrate board at different air velocities (2.5 m/s and 3.5 m/s). Higher velocities lead to faster heat dissipation from the IC chips, resulting in lower temperatures. IC chips experience a temperature reduction of 1.42%-17.33% at 2.5 m/s velocity compared to 3.5 m/s. The remaining 39 configurations exhibit similar trends. IC chip U2 generated the highest temperature in the arrangement owing to its small size and high heat build-up rate.

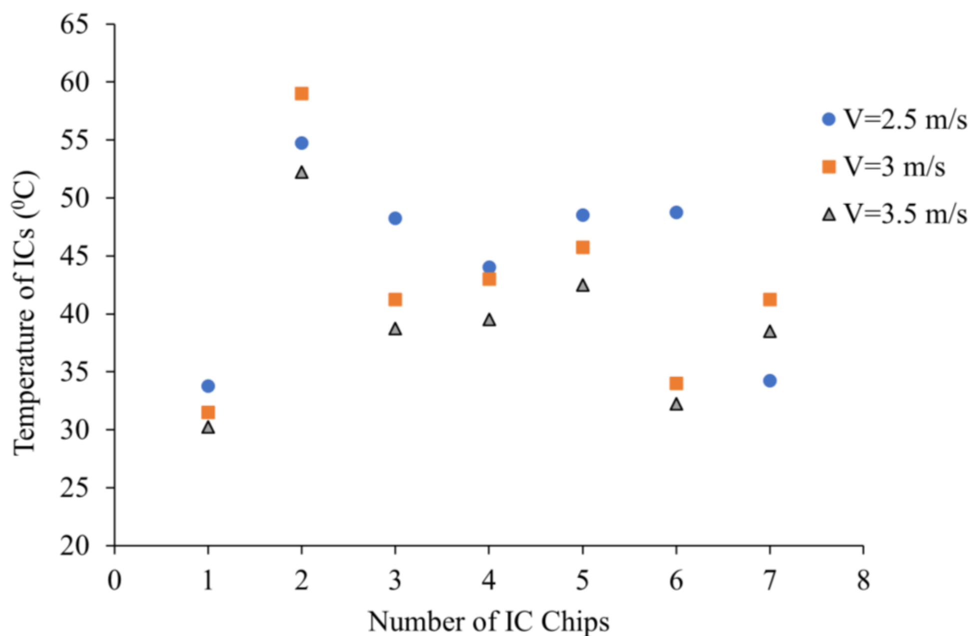

Fig. 6. Temperature variation of the IC chips of the horizontal board for different air velocities for λ = 2.17935

From the experimental method, it was evident that for higher values of λ, the average temperature of the configuration, heart transfer coefficient, and heat transfer rate were less, more, and more, respectively. The optimal configurations of ICs will be at higher values of λ; in this case, λ= 2.17935.

3.1 Implementation of Machine Learning Algorithms

Different linear regression models were used to predict average temperature values. The reason for selecting linear regression models over random forest is that linear regression may be preferred for extrapolation, owing to its simplicity, interpretability, and stability. The ability of linear regression to capture linear relationships in data makes it suitable for extrapolation beyond observed ranges, particularly when the underlying relationships are relatively stable. Its straightforward interpretation via coefficients aids in understanding extrapolated results. Additionally, linear regression tends to be less prone to overfitting than more complex models, ensuring more reliable extrapolation results, as mentioned by Hengl *et al.,* [32].

Figure 7 shows the prediction accuracy of the different algorithms implemented for the experimental results. The random forest algorithm yielded a higher accuracy. As shown in Figure 8, the average temperature predicted by the random forest algorithm does not follow the trend that the average temperature should decrease with an increase in velocity. The average temperature predicted by the linear regression algorithm followed the trend that the average temperature of the configuration decreased with an increase in velocity. Therefore, a linear regression technique was applied to the experimental data.

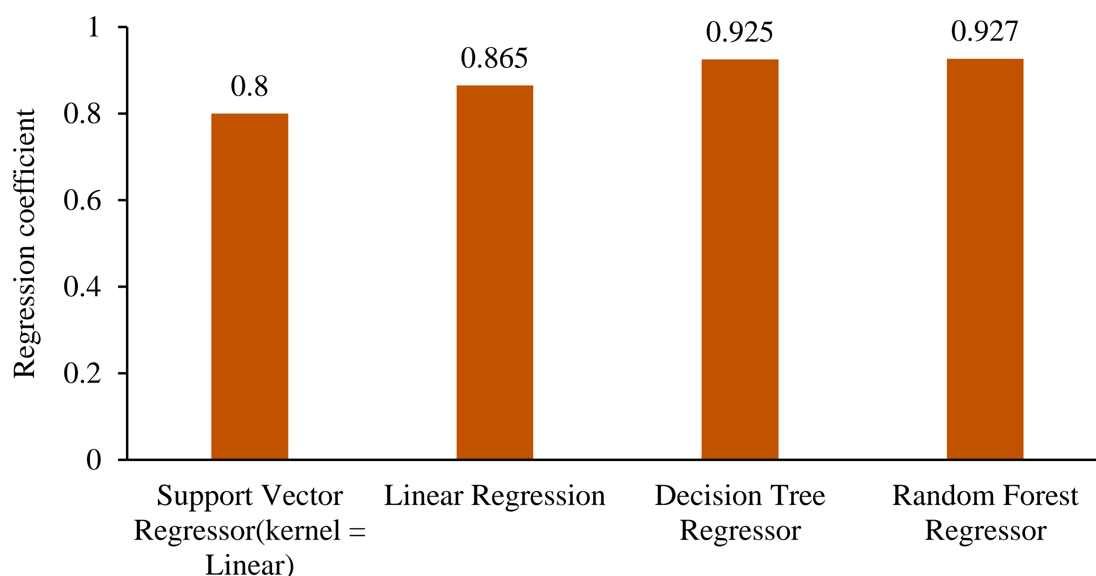

Fig. 7. Regression coefficient for different model

Figure 8 shows that the predicted average temperature of the ICs values decreased with an increase in velocity for linear regression, whereas for random forest, it was almost constant.

Figure 9 shows a comparison between the average temperature predicted by the linear regression algorithm and the experimental average temperatures for a velocity of 2.5 m/s. The maximum temperature variation in the average temperature of the configuration between the linear regression algorithm and experimental values was observed to be 3.41% for the configuration of λ = 2.1720.

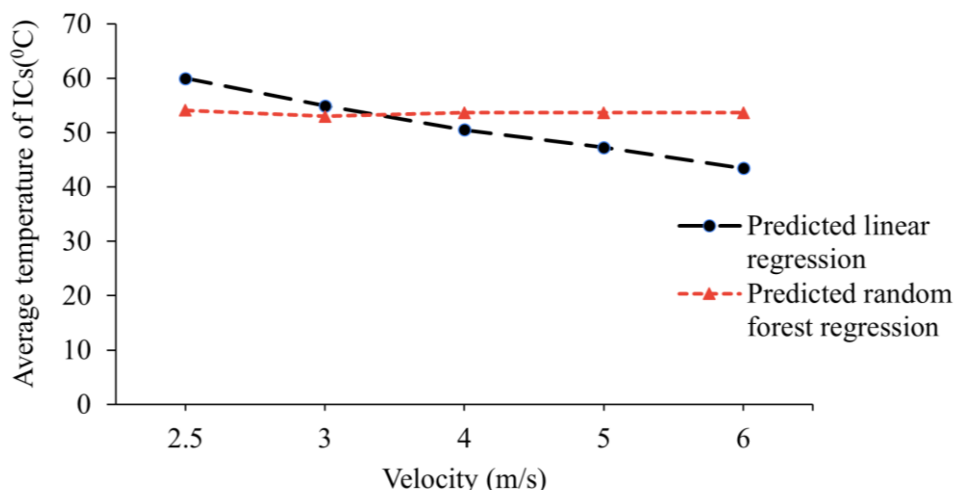

Fig. 8. Predicted average temperature from linear regression and random forest regression

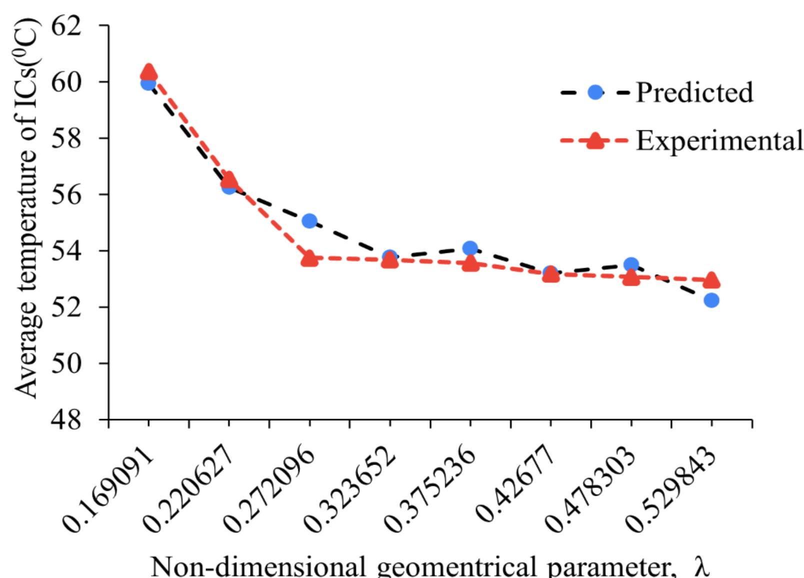

Fig. 9. Predicted v/s Experimental average temperature for velocity of 2.5 m/s

4. Conclusion

Steady-state experiments were conducted on seven asymmetric IC chips placed at various locations on a substrate board using the laminar forced convection heat transfer mode. The goal was to determine the ideal configuration of IC chips. The following conclusions were drawn from this investigation: The average temperature of the ICs decreases as the non-dimensional geometric parameter (λ) increases. The highest average temperature of the IC was at λ=2.17935. The heat transfer coefficient is highest at λ=2.17935, which corresponds to the minimum maximum temperature of the IC chips located at the lower border of the substrate board at the outlet section. The temperature of IC chips varies depending on their size, position on the substrate board, orientation, and heat flux. The smallest chip, U2, with a high heat buildup rate caused the highest temperature in the arrangement. The best design was determined by the nondimensional geometric distance parameter λ, which has the highest value at the lowest maximum temperature. A higher air velocity (3.5 m/s) resulted in a temperature reduction of 6.09%-14.02% compared to a lower velocity

(2.5 m/s) when cooling the IC chips. Different machine-learning algorithms were implemented for the experimental data, and linear regression algorithm was found to be suitable for the current data. The maximum error between the experimental and linear regression values was found to be 3.41%.

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