Simulation of Low Voltage DC-DC Booster Circuit with Improved Switch for Amplification of Biophotovoltaic Cell Output Voltage

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ARTICLE INFO	ABSTRACT
	Biophotovoltaic (BPV) cells otherwise called living solar cells are a clean energy-generating technology that uses photosynthetic organisms (cyanobacteria or microalgae) to produce electricity. However, the output voltage and current density of BPV cells are extremely low and the lifespan of BPV cells is short. In this article, a study based on computer simulation on the improvement of the switch of a low power DC to DC converter circuit is presented. A redesign of the circuit's switch (NMOSFETs) shows that a 10.5 % increase in output voltage is achievable with an increase in efficiency of 3.4 %. Simulation shows that the increase in performance is due to the very low ON resistance of the newly designed switch.

1. Introduction

Renewable energy sources today come mainly from wind and solar energy [1-3]. Biophotovoltaic (BPV) cells convert light energy into usable electrical energy by harvesting photo electrons excreted as by products from the photosynthetic activities of cyanobacteria and microalgae. The first BPV cells were demonstrated 40 years ago using *Rhodospirillum Rubrum*. They used a very simple setup where inert electrodes were used to harvest electrons from the organisms. Their system used the Indirect Extracellular Electron Transfer (IEET) where electron carriers diffuse between the sandblasted Platinum electrodes and the cells to produce a current density of 162 µA/cm^2 for 24 hours [4]. This type of system suffers from low power densities due to limitations in the rate of mass transport between the electrodes and the cells because the cells are contained in water, thus are mobile and not constantly in contact with the electrodes.

Recently, an abundance of work to further address this issue and to optimize the IEET type BPV cell is plentiful where innovative electrode designs, the use of bio-films to trap the organism and

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Redox Mediators to boost photosynthesis have helped to boost the power density. For example, in 2017, *Chlorella* was used in a semi-dry photosynthetically active bio-film entrapped in a 2 % Sodium Alginate gelatine and placed on an ITO anode. This *Chlorella* immobilization technique results in a higher rate of mass transport since the cells are in constant contact with the harvesting anode. The reported a power density was 0.289 mW/m^2 using an array of Red LEDs [5]. In 2019, it was demonstrated that the power density using the same setup can be increased to 0.456 mW/m^2 when illuminated using a light source that produced 150 µmol of photons/m^{-2}s^{-1}. It was also shown that higher photon counts will not produce more power [6]. In 2020, the same group of researches boosted the power density of the same setup to 0.58 mW/m^2 using a customized light source that possessed a spectral density that was closely matched to the absorption spectrum of the *Chlorella* algae used [7]. Apart from the use of algae, the use of Cyanobacteria species such as *Synechocystis sp.*, have also been demonstrated to produce a power density of 0.4mW/m^2. A ground breaking bio-electrode was developed by printing the bacteria using an inkjet printer onto paper [8]. In conclusion, modern BPV cells have shown an increase in power density. However, due to their nature of being living microorganisms, they quickly deteriorate causing the output power to degrade over a short period of time. BPV cells can sustain an output voltage for a limited number of days due to the use of living microorganisms in the cells. This period depends on the type of organism used in the cells. Thus, we believe that the energy produced by these cells should be maximized within this short time period. In this article, we propose a DC-DC Converter circuit designed for low input voltage range and is suitable optimizing the output energy from BPV cells.

The design of a DC-DC Converter to amplify the DC power of a single BPV cell initially sounds nontrivial, however considering the fact that the input power drive from a single BPV cell is very low, considerations to the selection of components for the circuit design is crucial. Moreover, a self-starting circuit is also required and has been demonstrated [9]. This paper addresses losses associated with the switch of the DC-DC Converter circuit and how it can be redesigned for low voltage input.

2. Switch Losses in Low Power DC-DC Converters

Among many electronic circuits, the use of a DC-DC Converter, shown in Figure 1 is chosen to amplify the output voltage of a BPV cell. It is thought to be the most suitable choice because it can be constructed mostly using only passive components which consists of an input inductor, *L*, a diode, *D*, an output capacitor, C_{out}, and R_{out}. However, Switch, *S*, requires fast toggling, thus it is typically implemented using a single solid-state MOSFET. Many designs have used an NMOSFETs to implement their switch [10,11].

The input is labelled as V_{in} while the output voltage, V_{out} is taken across the load/output resistor, R_{out}. In laboratory setups and industrial implementations, the switch is implemented using an NMOSFET that is toggled using a simple vibrator circuit, or even a microcontroller. Ideally, for a system fully powered by BPV cells, the NMOSFET toggling circuit would also have to be powered by an array of BPV cells. However, the design and management of the biological power supply for the toggling circuit will require much more investigation and is not discussed in this article.
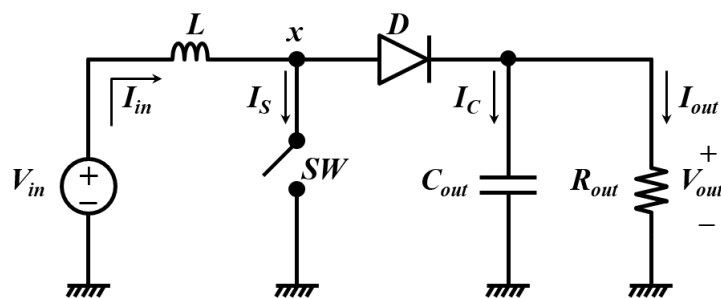
Fig. 1. DC-DC Converter Schematic

Among many parameters, it is noted that the efficiency, η of a DC-DC Converter also depends on the switch used. Two types of losses are inherent to this circuit when a single MOSFET is chosen to implement the switch. These losses are due to the MOSFET conduction loss and switching loss [12]. Both losses are associated with the finite ON resistance of the transistor. In one hand, we have conduction loss, caused by I^2R losses associated with the ON resistance of the transistor, and on the other hand, we have switching loss due to the finite amount of time for the switch to fully turn on. For example, the lower the ON resistance, the slower the turn on time of the switch. The slower the switch turns on, the higher is the switching loss and vice versa. Thus, this loss is related to the switching frequency, f_s [9].

To increase the efficiency of the circuit, the inefficiency of the switch should be decreased. This work concentrates on a simple modification of the switch such that the I^2R and switching loss can be reduced. The modification takes advantage of the closely matched parameters of NMOSFET switches fabricated using solid state technology and is explained in the next section.

3. Improving Switch Efficiency

The main leakages of power in a DC-DC Converter are inductor conduction losses, switch conduction losses and switching losses [13]. As mentioned earlier, in many cases, switch, S is implemented using an NMOSFET transistor. NMOSFET switches are fabricated using the CMOS process. A single design of the switch is replicated and fabricated on a single Silicon wafer, cut into dies, and finally packaged and distributed to the consumer. Since they are all fabricated on a single wafer, using a similar process, their mechanical and electrical variations are extremely small [14].

The NMOSFET as a switch works in two regions, which are the cut-off region when the switch is OFF, and the saturation region for when the switch is ON. When the switch is ON, the maximum drain current, I_D induced by the potential difference between the drain and the source flows through the device. This current is limited by the channel on resistance, where in the saturation region is denoted as R_{ON}. Thus, the NMOSFET can be modelled as a resistor between the drain and the source, as depicted in Figure 2.
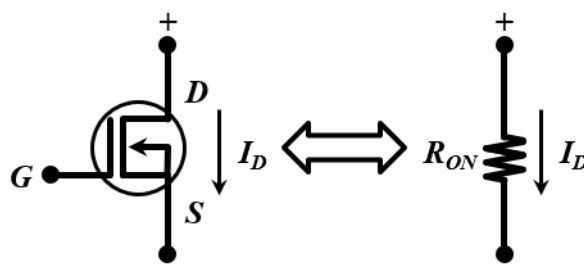

Fig. 2. NMOSFET in the saturation region

Although discrete NMOSFETs cannot be directly modified to decrease the value of R_{ON}, connecting two or more NMOSFETs in parallel can decrease R_{ON} because the resistance will be a parallel combination of the two NMOSFETs. Figure 3 shows the parallel connection of N number of NMOSFETs. Note that NMOSFET M_1, M_2 up to M_N have all of their respective gates, drains and sources tied together. If it is assumed that the transistors are perfectly matched and are all fully on, the drain current I_D, entering node D splits equally between all of the transistors and recombines upon exiting at node S. Note thar node D is at a higher potential than node S.
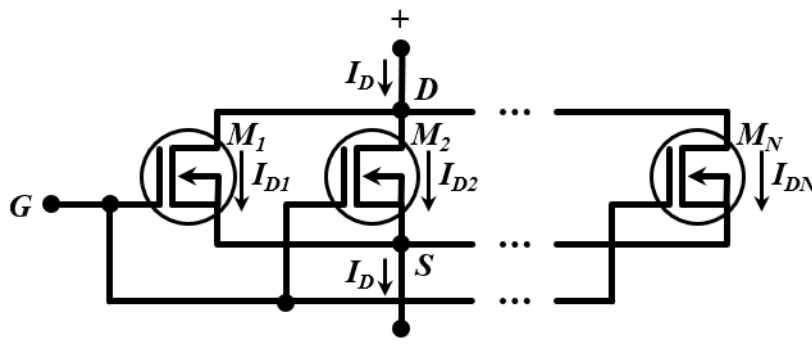

Fig. 3. NMOSFET parallel switch

The resistive network formed from the parallel switch configuration is therefore a parallel combination of each transistor's channel resistance. During the ON state of the parallel switch, the equivalent circuit is shown in Figure 4.
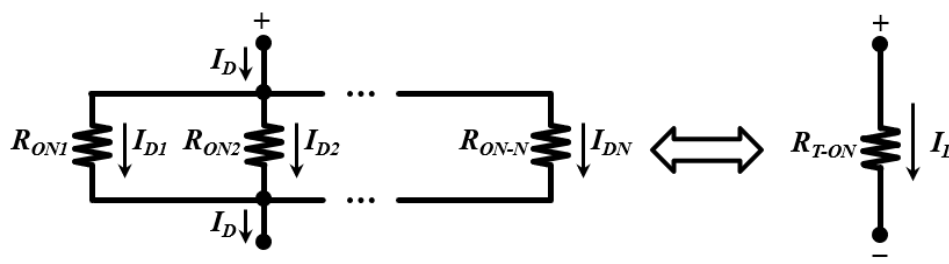

Fig. 4. NMOSFET parallel switch ON state equivalent circuit

The parallel combination of ON resistance can be modelled by a single resistor, R_{T-ON}. To find its value, we assume that all of the ON resistance of each transistor are perfectly matched. Thus, the reciprocal of R_{T-ON} is written as

$$\frac{1}{R_{T-ON}} = \frac{N}{R_{ON}}, \tag{1}$$

where N is the number of parallel connected transistors used to implement the switch. Thus, the reciprocal of Eq. (1) gives the value of the total switch ON resistance as

$$R_{T-ON} = \frac{R_{ON}}{N}. \tag{2}$$

In theory, an infinite number of transistors would cause R_{T-ON} to approach zero. Thus, during the ON state, zero current leaks to the ground and are channelled through the diode to charge the output capacitor in total. However, an infinite number of NMOSFETs to connected in parallel to form the

switch is impossible. Moreover, simulation shows that on a number of NMOSFETs should be sufficient to increase the output voltage gain to an optimum level.

4. Simulation of a Low Voltage DC-DC Converter for BPV Cells

The lowest R_{on} value of a discrete NMOSFETs is in the order of tens of milli ohms. A transient simulation was carried out in order to study the effects on the output voltage, voltage gain and efficiency when more than one NMOSFET in parallel is used to implement the classical single switch of a DC-DC converter. The input of the circuit is tuned to be similar to the low value of a single BPV cell. Our simulation was carried out using LTSpice XVII (x64). Figure 5 shows the schematic of the DC-DC converter using a single switch.
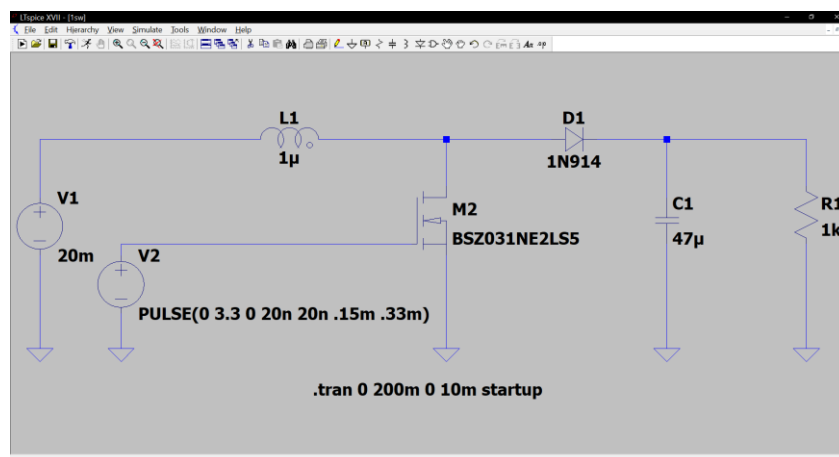

Fig. 5. DC-DC Converter with single switch NMOSFET

In our simulation, a constant voltage source, V1 is used as the input and was set to 20 mV in order to model the lowest voltage produced by a single BPV cell that we have recently produced [15]. We also note that for each simulation, the input power is set to 0.4 mW. This is done to model a $1m^2$ BPV cell as the input to our circuit. The internal series resistance of the voltage source in the simulation is set to 1 Ω in order to model the internal resistance of the BPV cell. The diode model used is the 1N914, a diode manufactured by ON Semiconductor. The output capacitor, C1 is set to 47 μF and the input inductor, L1 is set to 1 μH. An NMOSFET, M2 is chosen as the switch and is modelled using the BZS031NE2LS5 model file which also includes a 26 mΩ on resistance value. The switch is toggled by a 3.3 V pulse with a 50 % duty cycle running at rate of 3 kHz. A transient simulation was executed for 200 ms and the output voltage is probed across a 1 kΩ output resistor, R1 and ground.

Figure 6 shows the output voltage produced when a single switch is used. At the end of the simulation, the output levels to approximately 246 mV with a 249 μA current flowing through R1, delivering approximately 61 μW of output power. The input power obtained from the simulator is 0.4 mW on average. Thus, the efficiency of the circuit using a single switch is approximately 15.3 %.
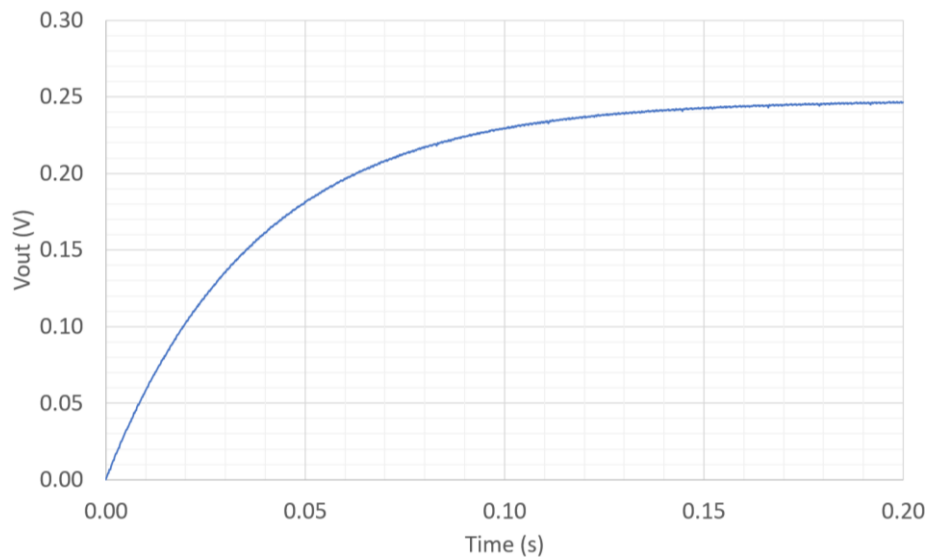
Fig. 6. Single switch output voltage

Another NMOSFET, M3 was added in parallel with M2 to simulate the use of a similar parallel transistor as seen in Figure 7(a). The same simulation and analysis were carried out and they were results recorded. The process of adding parallel NMOSFETs into the simulation schematic followed by circuit simulation and result recording was carried out until finally six NMOSFETs were connected in parallel to form the switch as shown in Figure 7(b). The output voltage is shown in Figure 8.
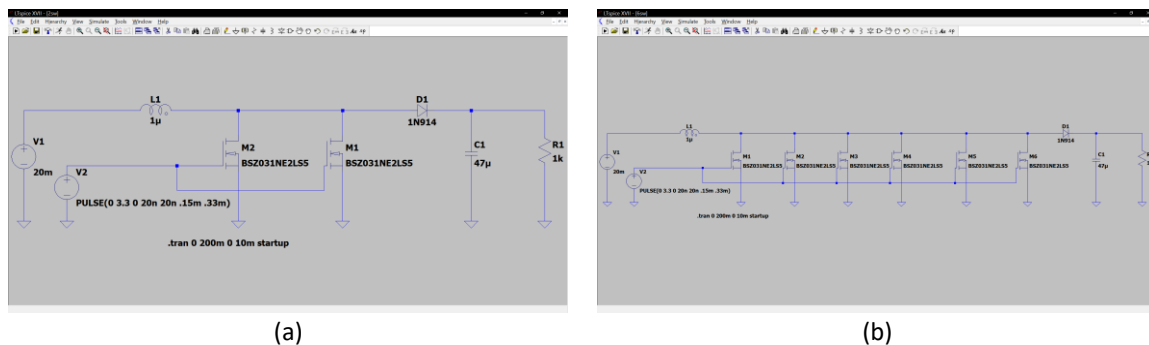

(a)

(b)

Fig. 7. DC-DC converter input schematic for (a) 2 parallel switches, (b) 6 parallel switches

The simulated output voltage produced by using 1 to 6 parallel switches are superimposed and in Figure 8. The output of using 1 parallel switch is labelled as VP-1. The labels VP-2, VP-3, VP-4, VP-5 and VP-6 are the output voltages when 2, 3, 4, 5 and 6 parallel switches are used. At the end of the simulation, it is observed that as the number of parallel switches increases, the output voltage also increases. For example, VP-1 reads 246 mV when only a single NMOSFET is used and VP-6 reads 275 mV when 6 parallel NMOSFETs are used.
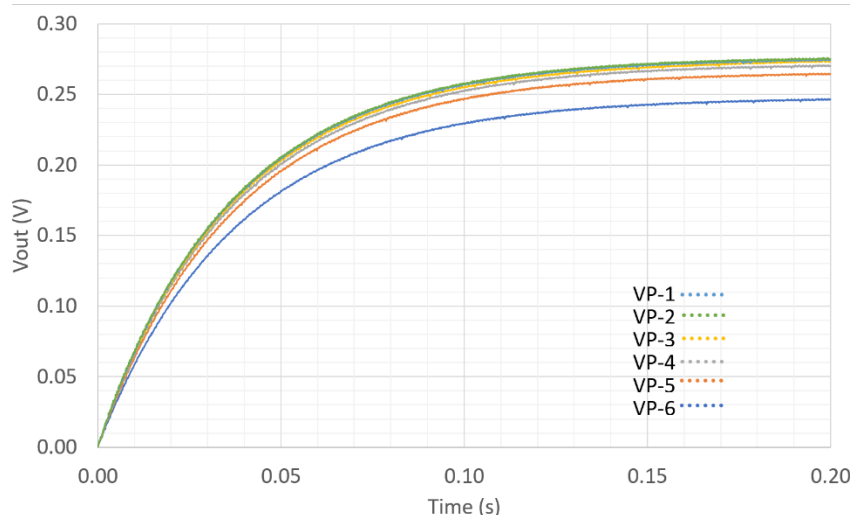
Fig. 8. DC-DC converter output voltage for 1 to 6 parallel switches

Figure 9 is a plot of the output power delivered to the output resistor, *Rout* (see Figure 1) when 1 to 6 parallel NMOSFETs are used as its switch. It is observed that the output power increases from 60 μW when 1 switch is used to approximately 75 μW when 6 switches are used. However, simulation results suggests that the power saturates at 75 μW even if more parallel NMOSFETs are connected as the switch. This also suggests that the efficiency of the circuit saturates as the number of parallel NMOSFETs are increased.
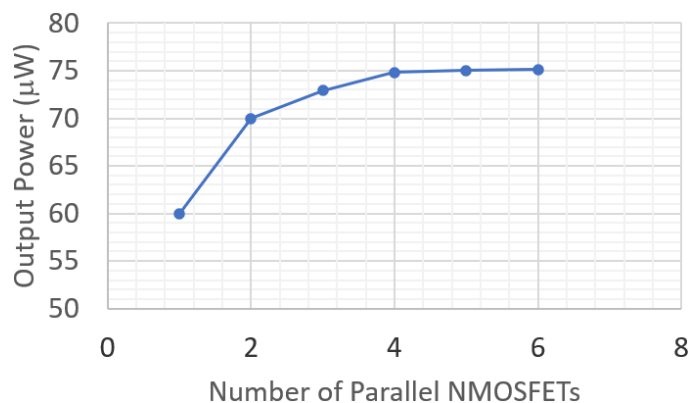
Fig. 9. Output power versus number of switches

Figure 10 shows a plot of the number of parallel NMOSFET switches used to implement the switch as a function of the efficiency of the DC-DC converter. The efficiency is obtained by dividing the output power by the input power which is on overage 0.4 mW as described earlier in this section. When only a single NMOSFET is used, the efficiency is 15.5 % and increases to 18.9 % when six NMOSFETs are used. The shape of the plot shows the saturating effect on efficiency as the number of parallel NMOSFETs increases.
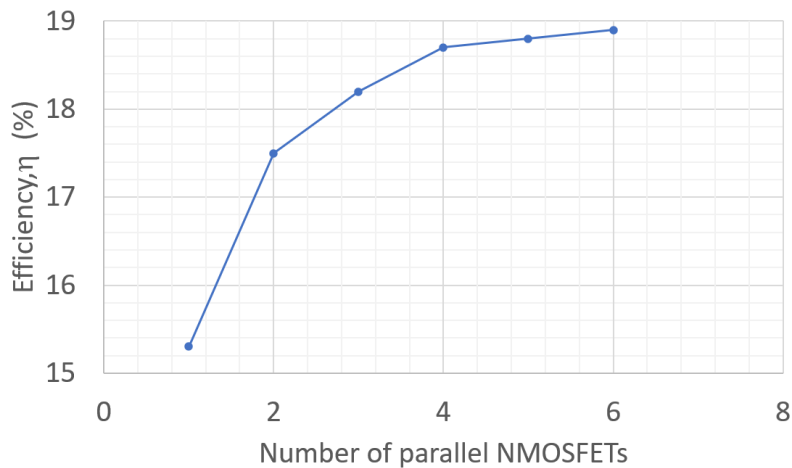
Fig. 10. Number of parallel NMOSFETs versus Efficiency

The next section discusses the main cause of saturation of power and efficiency when the number of parallel switches used is increased.

5. Efficiency Saturation

According to Eq. (2), the ON resistance of the switch decreases as more parallel NMOSFETs are connected together. Plugging in 2.6 mΩ as the ON resistance of a single MOSFET used in our simulation, it is observed in Figure 11 that the switch ON resistance decreases and approaches zero as more NMOSFETs are used to implement the switch.
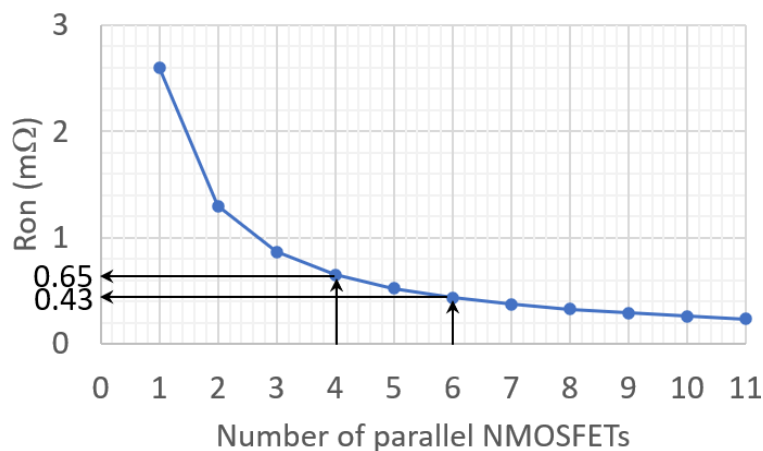
Fig. 11. Switch ON resistance versus number of NMOSFETs

A significant decrease in ON resistance occurs when 4 to 6 parallel NMOSFETs are used. From the plot, when 4 transistors are used, RON drops to 0.65 mΩ, and to 0.52 mΩ and 0.43 mΩ 5 and 6 transistors are used, respectively. The average drop in resistance is approximately 80 % in between these values. There is an insignificant decrease in resistance when more than 6 switches are used.

It is also observed that the shape of the plot is a mirror image of the plots of power and efficiency in Figure 9 and Figure 10, respectively. This shows a strong correlation between output power, efficiency the ON resistance of the switch. During the switch ON time, the input current passing through the switch, I_S of the DC-DC converter (Figure 9) is equal to V_X divided by the ON resistance of the switch. When using the proposed parallel switch method, the switch current is given by

$$I_S = \frac{V_X}{R_{T-ON}}. \tag{3}$$

By substituting Eq. (2) for $R_{T\text{-}ON}$ into Eq. (3), the DC switch conducting current is written as

$$I_S = \frac{NV_X}{R_{ON}}. \tag{4}$$

This shows that the switch is able to conduct N times more current to ground when it is turned ON. On the other hand, the effects of using parallel transistors also causes the drain-source resistance, R_{DS} to decrease. By similar analysis with calculating $R_{T\text{-}ON}$, the total drain-source resistance, $R_{DS\text{-}T}$ is given as

$$R_{DS-T} = \frac{R_{DS}}{N}. \tag{5}$$

From Eq. (5), we see using many parallel connected transistors decreases $R_{DS\text{-}T}$. The value of R_{DS} should be very large in order to minimize the magnitude of leakage current flowing to ground when the switch is OFF. Thus, the downside of using parallel connected transistors is that the total R_{DS} value also decreases, thus increasing the magnitude of leakage current to ground when the switch is OFF. This causes the efficiency to saturate as N increases.

The effects the switch current can be seen in the simulations. Figure 12 shows 6ms of the transient current through the switch for when (a) a single transistor versus (b) 6 transistors are used as the switch. In both plots, I_{ON} designates the switch current values when the switch is ON and I_{OFF} for when the switch is turned OFF. It is observed that in both figures, when the switch is turned ON, the current rises to approximately 450 mA for the single transistor switch and only to 80 mA when 6 transistors are used. This is attributed to the decrease in $R_{T\text{-}ON}$ from 2.6 mΩ to 0.43 mΩ for a single transistor switch to a 6-transistor switch configuration. A large switch ON current, $I_S=I_{ON}$ that flows from the inductor to ground of the DC-DC converter (see Figure 1) allows for a more efficient discharge of the diode capacitance and overall a much efficient circuit.
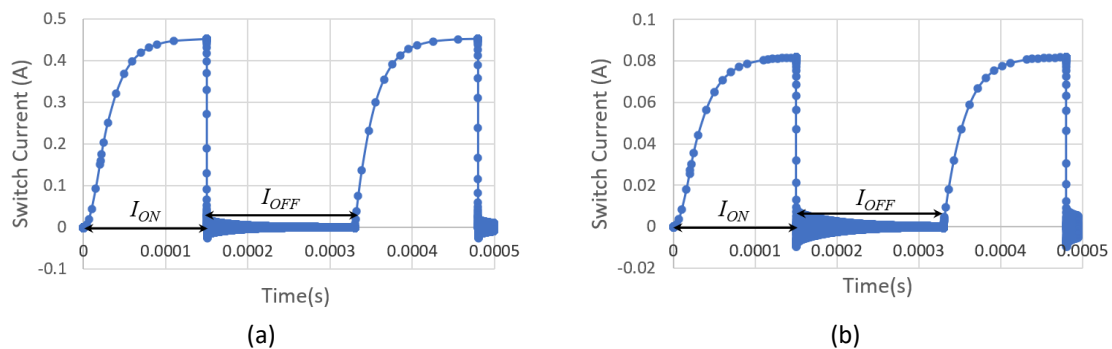
Fig. 12. Simulated current pulses for a (a) 1 transistor switch, (b) 6 parallel transistors switch

On the other hand, when the switch is OFF, both figures show a value that is almost zero for the switch current (I_S in Figure 1). However, detailed analysis of only the I_{OFF} currents reveal that it is approximately on average at -0.15 mA for figure 12(a) and -0.11 mA for figure 12(b). The increase in leakage current (I_{OFF}) is attributed to the decrease in $R_{DS\text{-}T}$. Ideally $R_{DS\text{-}T}$ should be infinitely large. This would allow the switch to direct all of the input current, I_{in} to flow through the inductor and diode to the output capacitor of the DC-DC Converter (see Figure 1). From our simulations for switches

implemented using 1 to 6 transistors, I_{OFF} is finite and decreases as the number of transistors are increased.

Figure 13 shows plots of the average magnitudes of I_{OFF} and I_{ON} for different N values in subplots (a) and (b), respectively.
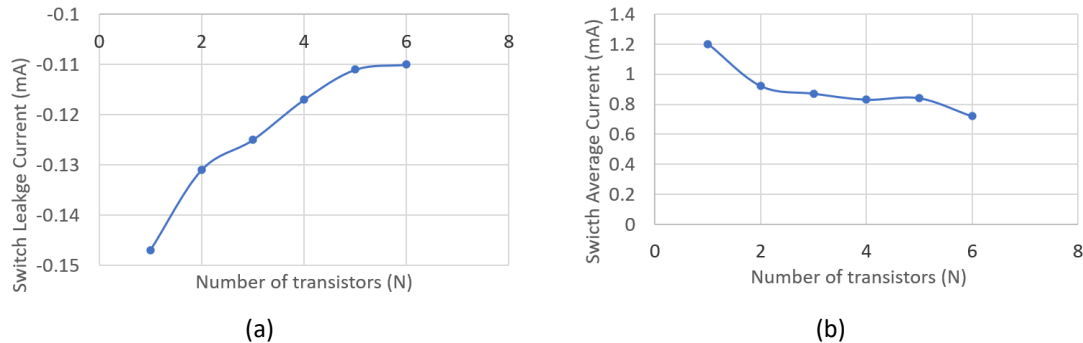

(a)   (b)

Fig. 13. Switch average currents versus number of parallel connected transistors (a)

Both plots show that as the number of transistors is increased, both the average ON and OFF currents also increase and is attributed to the decrease in the total drain source resistance of the switch when it is ON and decrease in transistor ON resistance when the switch is OFF.

6. Conclusion

For low input DC-DC converters targeted to maximize the output of BPV cells, the implementation of 6 parallel connected transistors as the switch has shown to increase the output voltage by 10.5 %. This is a significant boost in output voltage that can be fed into a second stage to boost the voltage up even further. On the other hand, the boost in efficiency is only 3.4 %, which is due to the increase in leakage current as the total drain source resistance decreases when 6 parallel transistors are used as the switch. In order to further increase the efficiency, a two stage DC-DC converted may be designed where the second stage also uses parallel connected transistors as its switch.

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