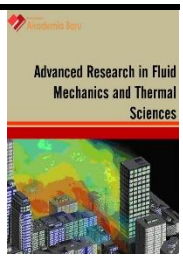
Penerbit Akademia Baru

Journal of Advanced Research in Fluid Mechanics and Thermal Sciences

Journal homepage: www.akademiabaru.com/arfmts.html
ISSN: 2289-7879



Study of Thermal-Fluid Analysis on Fusible Metal Bonding Application

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ARTICLE INFO

Article history:
Received 16 December 2018
Received in revised form 2 July 2019
Accepted 13 September 2019
Available online 13 October 2019

ABSTRACT

Due to the rapid growth of wireless communication systems, high frequency packages become very important and they require compactness, low cost and high performances. Flip-chip assembly using organic substrate at very high frequency has become a cost competitive packaging method in semiconductor industries.Copper pillar interconnects are a popular interposing option due to the advantages of small pillar size and good thermal and electrical performance, making copper pillar interconnects very useful for high-frequency and high-density flip-chip packages. However, the challenges associated with the technology include controlling the formation of intermetallic compounds (IMC) and weak interfaces during heat-related processes. This paper discusses the influence of various temperature bonding on copper pillar solder joints reliability by using flip chip device. Testing on the flip chip samples will be tested and to determine the failure analysis of flip chip bonding after hot reflow process. The test results show that the interconnection of copper pillar can effectively be improved by controlling the temperature setting of the bonding process. The basic requirements of the joining material and the process will be discussed in this study.

Keywords:
Thermal-Effect; Fusible Metal Bonding; Flip-Chip

1. Introduction

A fusible metal is a metal alloy capable of being easily fused and melted, at relatively low temperatures. They are commonly known as eutectic alloys, and in this sense are widely used for eutectic solder with low cost and good properties in fusible metal bonding application, especially in flip chip packaging. Flip chip packaging is a method for interconnecting semiconductor devices to external circuitry with copper pillar solder interconnection that have been deposited onto the chip surface pads. The first flip chip was introduced by IBM in the late 1960's is known as Controlled Collapse Chip Connection (C4) [1, 2]. In contrast to the through-hole packaging that involves the use of leads on the components that are inserted into printed circuit boards' holes, the metal alloys

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copper pillar solder nowadays are deposited on the chip pads on the top side of the wafer during the final wafer processing step of the flip chip process. In order to mount the chip to the external circuitry of a circuit board, it is flipped over so that its top side faces down, and aligned so that its pads align with matching pads on the external circuit, and then the solder is reflowed to complete the interconnect. Flip chip metal alloys have the highest melting point possible where the temperature at which the material is solid is equal to the temperature at which the material is liquid. Flip chip alloys begin to melt at one temperature and then enter a slushy state before they fully melt at a higher temperature. Low or high melting alloys are available in a variety of forms such as cake, ingot, bar, shot, wire, stick, strip and custom shapes. In addition to this, low manufacturing cost able to be gained through lead frame density and speed optimization on flip chip. Lead frames are the metal structures inside the flip chip package that carry signals from the die to the outside. High chip to lead frame density and die bond process elimination on flip chip products are dominant advantages for material and speed improvement. Figure 1 shows the flip chip back side sample and Figure 2 shows front side of flip chip sample. Figure 3 shows the bonding process of flip chip samples on the surface of lead frames bond pad with respect to heater temperature control.

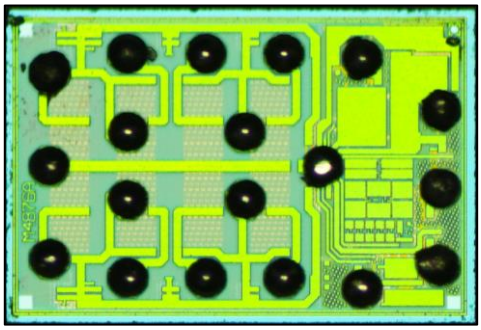


Fig. 1. Back side flip chip sample

Fig. 2. Front side flip chip sample

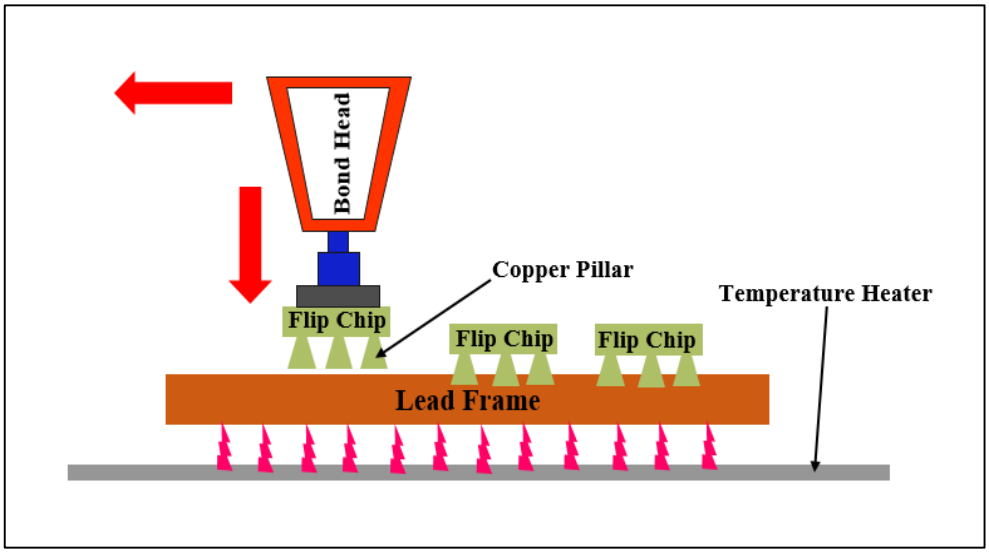


Fig. 3. Flip chip bonding process

1.1 Packaging Performance

In terms of packaging performance, flip chip is able to shrink down the die size to package size ratio beyond today wire bond package capability. Along with the growth of flip chip technology, copper pillar solder joint robustness is a concern topic that frequently being raised and discussed

nowadays. The performance and reliability of the devices are strongly dependent on the quality of the die-attach layers. It is always expected to make the die-attach layers as free of voids as possible since the voids are poor thermal and electrical conductors and also are stress concentration centers. There are three major causes for void formation, which include poor solder wetting due to surface oxides, vapor out-gassing by flux decomposition, and gas entrapment from preform melting. It is known that the gas entrapment is more significant for larger dies and can be managed by gas evacuation before the melting of the solder. However, a good flux less and oxide-free technology for metal die attach is still lacking. The organic fluxes used in conventional soldering not only induce void formation but also leave residues, which contaminate the dies and are corrosive. In addition to being costly and inconvenient to clean, the residues at the bonding interfaces of the die-attach layer are trapped, thus degrading interfacial bonding over time. The high density flip chip lead frame uses diffusion bonding, flux less and reflow less. To achieve a reliable interconnect there are certain criteria's that need to be met and controlled where no excessive heating as this would weaken the joints minimum 3um fusible metal thickness on lead frame so that the joint don't have course grain formation during diffusion bonding. As an error proofing method to avoid the dies from sitting on the bonding zone heater block for too long, which will weaken the joint formation, few method are implemented which is auto indexing feature whereby the lead frame would auto index certain number of columns if the time limit is breached. A study conducted by Nadlene [3] showed that the depth penetration of Cu-based lead frame decreases when the hardness is increased. They also found that voids formation had occurred at 180^{o}C and became worse when the temperature was further increased. Sangil *et. al* [4] found out that the chemical reaction between solder and underfill during the solder wetting and underfill cure process has been found to be one of the most significant factors for void formation in high input output and fine-pitch flip chip in package assembly using no-flow underfill materials.

1.2 Studied on Reflow Profile

A paper by Suraski [5] presented regarding on the theoretical condition of (RTS) Ramp-to-Spike of reflow profile temperature. The study recommended a Ramp-to-Spike reflow profile temperature in absence of soak zone. Soak zone can be describe that the function to minimize a huge gradient of temperature across the reflow system so that all the inner parts and materials of assembly is heated steadily and gradually. This result that reflow profile implemented can be design and used in the latest develop reflow oven such as conventional oven. This convention oven are able to maintain the heat to an assembly material steadily and uniformly. In addition that there are few advantages of RTS reflow profile for previous back traditional reflow profile such as brighter and shiner joints, wetting and solder ability issues. Weicheng [6] investigated that the formation of void percentage during reflow soldering of BGA device. The study indicates that with the presence of solder joints, void are very easily produced and formed during hot reflow bonding process. The formation of voids in solder joint is the main most demanding factor that controlling the solder joint performance and reliability. In addition, voids formation may lead to weaken the mechanical robustness of the interconnection level of board and therefore affect the performance of reliability. In the study states that in order to reduce voids formation in the solder joint process during soldering reflow of BGA device bonding process, the aspect that need to be considered is the reduction of oxide compound in the solder composition and metallization of substrate. It can be concluded that latest reflow vacuum technology with the present of vacuum system is proposed to have good voids percentage for free soldering and void free.

1.3 Intermetallic Compound Concept

In general, intermetallic compound or knows as IMC layers are form at the beginning of the process as parts of wetting process during reflow by the molten solder. Hence, the process can be expanded further by solid state point process changing of solder joint and cooling process or solidification process. Studies show that the solid state expansion rate increases with the presence of temperature parameter and time duration. Besides that increasing the diffusion rate, intermetallic compound expansion rate can be reduce when the reaction and behavior of IMC is consistent such as Cu-Sn is fully saturated during reflow process. In the formation of intermetallic layer such as copper, tin and silver can be illustrate that the formation of metallurgical bonding between the hot molten solder and the surfaces of the pad. One of the influence aspect which the influence on joining material solder joint reliability can be determine by the formation of intermetallic compound layer (IMC) between hot reflow melting solder and surface substrate of the interface. The existence of intermetallic compound layer represent a good metallic bonding during reflow but in another hand the intermetallic compound layer is also known as the weakest and failure parts in joining materials if the joint is brittle and frangible. A thick formation of intermetallic compound layer will degrade and weaken the joint. This weaken joint will have less able to withstand when subjected to the thermal loading cycling and strain operating demand on solder joint during time. Due to the outstanding of IMC, studies and investigation on the effect of intermetallic compound joint reliability have been a great demand of study in the manufacturing industry. The investigation reported in this studies on the formation of intermetallic compound in solder joint materials explained that most of the research have conducted and focused on the dissolution rate of metal substrate into the hot reflow molten solder. It can be observed that the formation intermetallic compound between the solder alloys and substrate surface of pad following the solder alloy pattern. Moreover, there is not much of interest on research experimental on the effect of surface pad sizes in the intermetallic compound layer thickness. [7-15].

2. Methodology

2.1 Sample Preparation

Sample of chip bonding under different temperature loading will be used in this study. The general description for the flip chip die bonding process is to pick up the chip from the flip sawn wafer and then to apply thermal temperature bonding to form intermetallic compound formation between copper pillar solder and lead frame die pad. Poor wetting and solder joint crack are the most common manufacturing defects for flip chip. On top of the difficulty to detect through optical inspection and x-ray, such defects also not able to be screen out effectively through tighten test limit. Thermal mechanical stress induced during reflow aggravates the solder joint crack and fails during electrical testing. The temperature is controlled by using heater block where the substrate will heat up following the setting temperature. Thus, this paper presents the effect of thermal loading on the intermetallic compound of copper pillar solder for fusible metal bonding application. Figure 4 shows the position of lead frame after enter heater block area. Figure 5 shows the position and bond head ready to pick up flip chip die on the wafer and Figure 6 shows bond head with flip chip die bonded on the surface of pad of hot temperature. Table 1 shows temperature setting for 280^{o}C parameter and Table 2 shows temperature setting for 290^{o}C in this experiment. The heater block heating will follow step by step processes before reaching the peak temperature as previously set for the experiment.

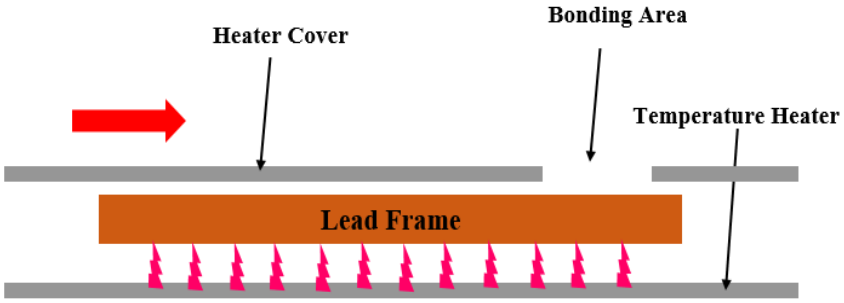


Fig. 4. Position of lead frame inside heater temperature

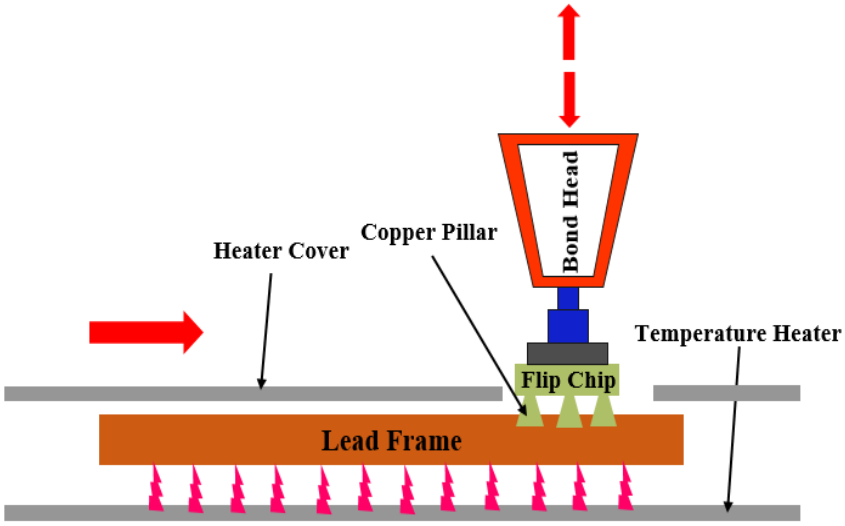


Fig. 5. Position of bond head ready to pick up flip chip die on wafer

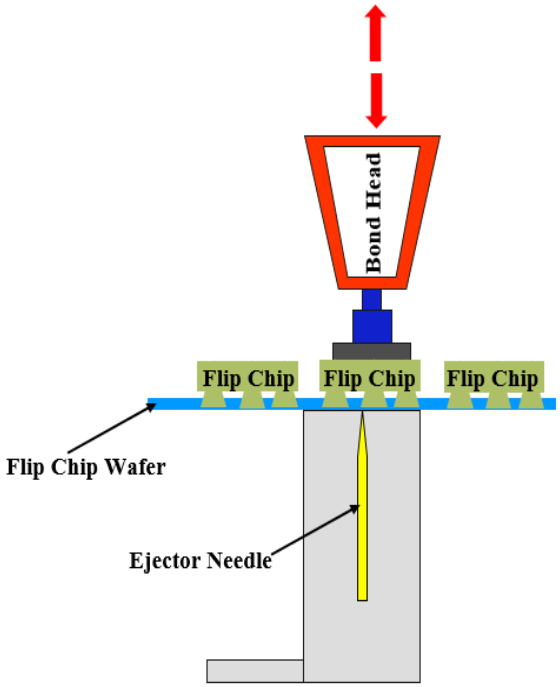


Fig. 6. Bond head pick up and bond on the surface pad of lead frame

2.2 Samples Preparation for Experiments and Parameters Setting

Table 1 and 2 shows the temperature setting that will be used in this experiment. Table 3 shows the parameters and setting value for the flip chip bonding in this study. A total 120 units of flip chip sample will be used in this experiment with respect to temperature setting. For the first experiment, 80 units bonded flip chip will be examined using die shear test with 280^{o}C and 290^{o}C and the observation of the thickness of the copper formation will be conducted by using a Scanning Electron Microscope (SEM). In the second experiment, 40 units of bonded flip chip will undergo cross section area and observation on the copper pillar interconnection will be conducted by using Scanning Electron Microscope (SEM).

Table 1
Temperature setting for 280^{o}C

Zone	Temperature Setting (^{o}C)
Pre-Heat 1	150
Pre-Heat 2	200
Pre-Heat 3	240
Bonding Front	280
Boding Rear	280
After Stage 1	150
After Stage 2	100
After Stage 3	80

Table 2
Temperature setting for 290^{o}C

Zone	Temperature Setting (^{o}C)
Pre-Heat 1	150
Pre-Heat 2	200
Pre-Heat 3	240
Bonding Front	290
Boding Rear	290
After Stage 1	150
After Stage 2	100
After Stage 3	80

Table 3
Parameters and setting for flip chip bonding

Temperature Setting	Staging Time	Number of Samples	Purpose
280^{o}C/290^{o}C	No Staging time	30 units	Die shear Test
280^{o}C/290^{o}C	No Staging time	30 units	Die shear Test
280^{o}C/290^{o}C	No Staging time	10 units	X cross Section
280^{o}C/290^{o}C	No Staging time	10 units	X cross Section
280^{o}C/290^{o}C	10 second	10 units	Intermetallic Compound Observation
280^{o}C/290^{o}C	5 minute	10 units	Intermetallic Compound Observation
280^{o}C/290^{o}C	10 minute	10 units	Intermetallic Compound Observation
280^{o}C/290^{o}C	15 minute	10 units	Intermetallic Compound Observation

2.3 Sample Characterization

2.3.1 Die shear test

Die shear test is used in this experiment to observed the formation of copper pillar solder on the surface of pad after flip chip bonding. Figure 7 shows the Dage 4000 Bond tester machine used for die shear test in the experiment. Figure 8 shows the shear tool position for the tool to push the die from the surface of the pad and Figure 9 shows the location area of copper pillar of die after shear.

Fig. 7. Dage 4000 bond tester

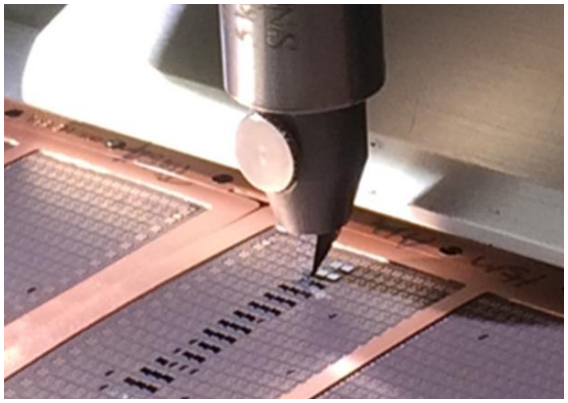


Fig. 8. Shear tool positioning

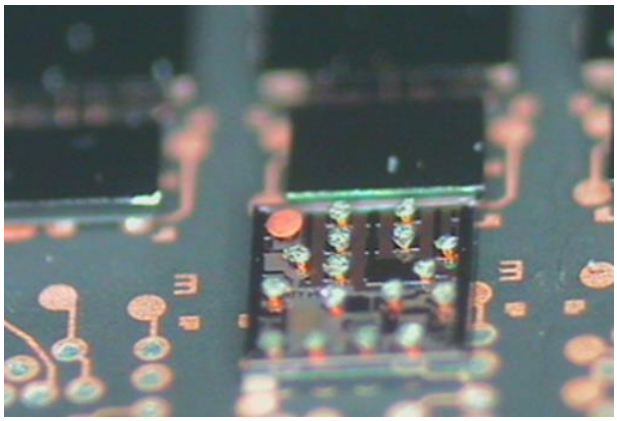


Fig. 9. After shearing process

Figure 10 shows the die shear contact angle where the contact tool will push the units after samples fully bonded on the surface of the pad. Table 4 shows the shear mode description after shear test. The mode indicates the behavior of copper pillar melted on the surface pad after reflow. This mode helps to determine in which mode the copper pillar belongs after shear test following the specification limit of the flip chip package.

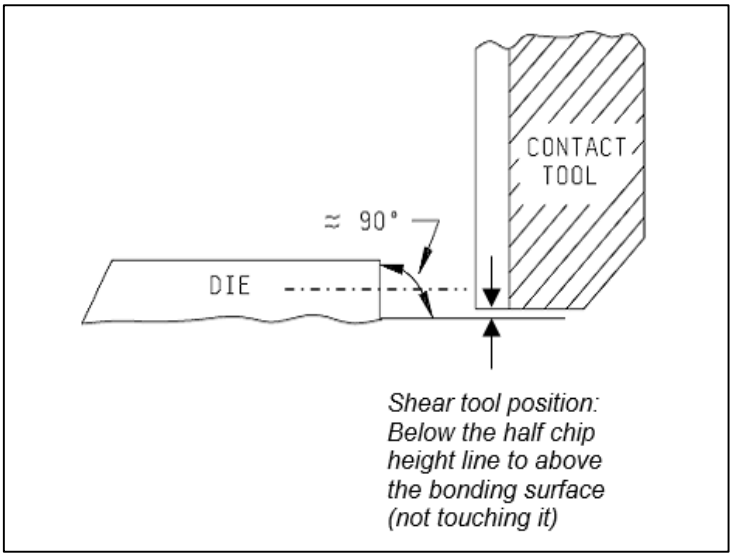


Fig. 10. Die shear contact angle

Table 4
Shear mode description

Shear mode description	Mode	< Spec Limit	≥ Spec Limit
All pillars break @ lead/circuit pad	1	Fail	Pass
All pillars break @ chip pad	2	Fail	Pass
Pillars mix break @ lead & chip pads	3	Fail	Pass
Missing pillar or solder	4	Fail	Fail
Break with lifted circuit pad	5	Fail	Pass
Solder bridging	6	Fail	Fail
Insufficient solder coverage (<25%)	7	Fail	Fail
Insufficient solder compression	8	Fail	Fail

2.3.2 Scanning electron microscope (SEM)

SEM is an important tool for analysis semiconductor die failure analysis as well as metallurgical failure analysis. SEM can provide detailed image of up to 120,000X magnification with typical magnification of 50,000X to 100,000X, resolve features down to 25 Angstroms. With a SEM image, the depth of field is fairly large, providing a better overall three-dimensional view of the sample. SEM examinations are often used to verify semiconductor die metallization integrity and quality. Figure 11 shows Scanning Electron Microscope (SEM) used in the Faculty of Mechanical Engineering, Universiti Teknikal Malaysia Melaka (UTeM). Figure 12 shows the schematic design of Scanning Electron Microscope (SEM). The Scanning Electron Microscope will be used in this experiment to observe the formation of the intermetallic compound and the copper pillar legs in the cross section area examination.

Fig. 11. Scanning electron microscope (SEM) at UTeM

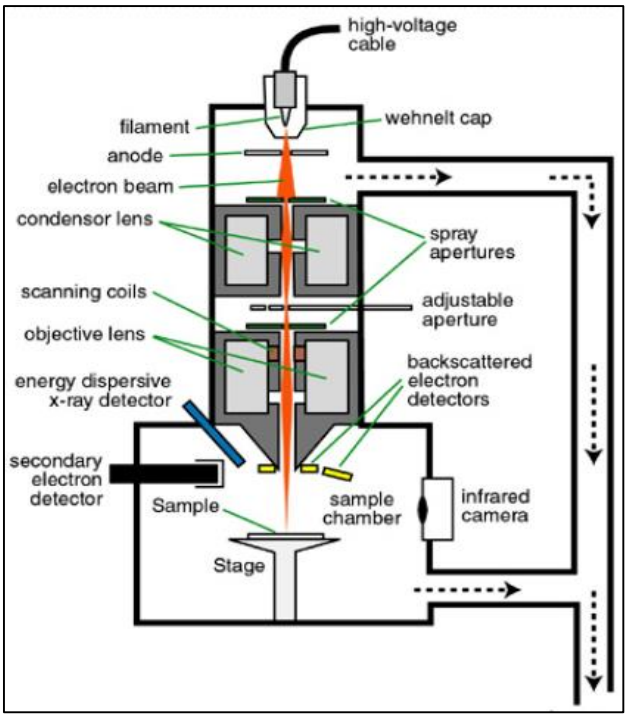


Fig. 12. Schematic design of a SEM

3. Results and Discussions

3.1 The Formation of Copper Pillar Solder with Various Temperature after Die Shear Test

3.1.1 Solder melting at 280^{o}C and 290^{o}C

As shown in Figure 13, it can be seen that the solder amount that sticks at the location of the bonding pad area is not thick enough at 280^{o}C. This is because the temperature set at 280^{o}C is not providing enough heat to make sure that the solder at the chip will be melted on the location of the pad. It can be observed that, the edge corners have low amount of solder that sticks on the area of the pad compared to the location at the center of the pad. Based on the image in Figure 14, it can be seen that the solder amount that sticks at the location of the bonding pad area is equally thick enough at 290 ^{o}C. This is because the temperature set at 290^{o}C provides enough heat to make sure the solder at the chip melted on the location of the pad center and every edge. It can be observed that, every

corner of the edges has equal amount of solder stick on the area of the pad and at the center of the pad. The amount of solder melted is thick enough at 290^{o}C to make sure that the chip is fully bonded on the pad location.

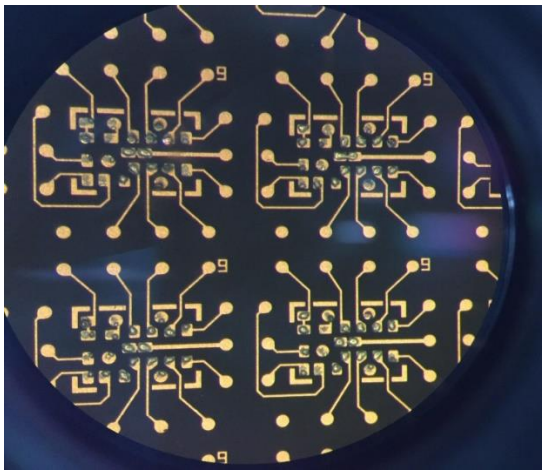


Fig. 13. Die shear test at 280^{o}C sample

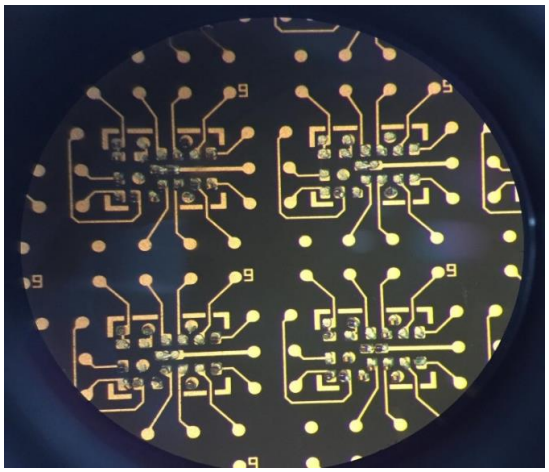
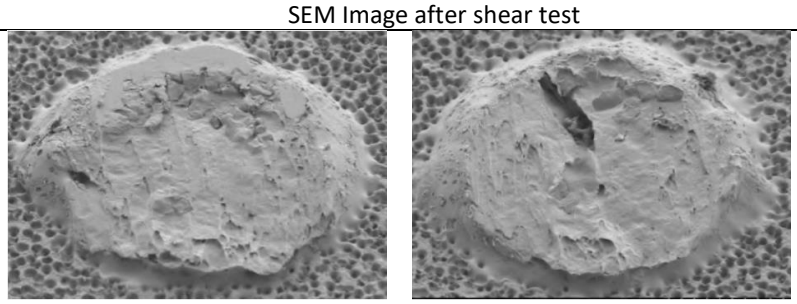
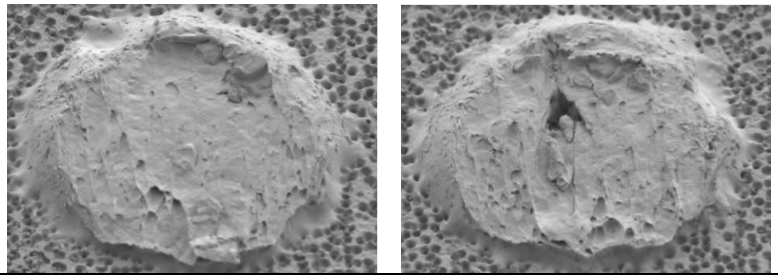


Fig. 14. Die shear test at 290^{o}C sample

3.1.2 SEM image after shear test

Table 5 shows the formation of copper pillar solder after die shear test. It can be seen under SEM images for 280^{o}C and 290^{o}C bonded units. Several surface pads are seen under SEM images as shown above. It can be concluded that the surface of copper pillar after die shear test looks thicker for both temperatures. It can be seen that the copper pillar sticks and harden simultaneously on the surface of pad. This can be concluded that, the surface of copper pillar after die shear test shows an even formation of copper surface. It can also be observed that there is no crack of copper around the surface of copper bonded on the pad.

Table 5
Copper solder formation using SEM image after shear test

Temperature sample	SEM Image after shear test
280^{o}C	
290^{o}C	

3.1.3 Die shear test value of sample

Figure 15 shows the die shear test value versus bonded units at 280 °C. Total of 30 samples of flip chip units were bonded at 280°C. From the Figure 15 it can be observed that the maximum die shear value is 799.9gmf and average value of die shear is above 700gmf. Besides that, the minimum die shear value observed is 564.3gmf. The overall units are within in the border of lower control limit (LCL) and upper control limit (UCL).

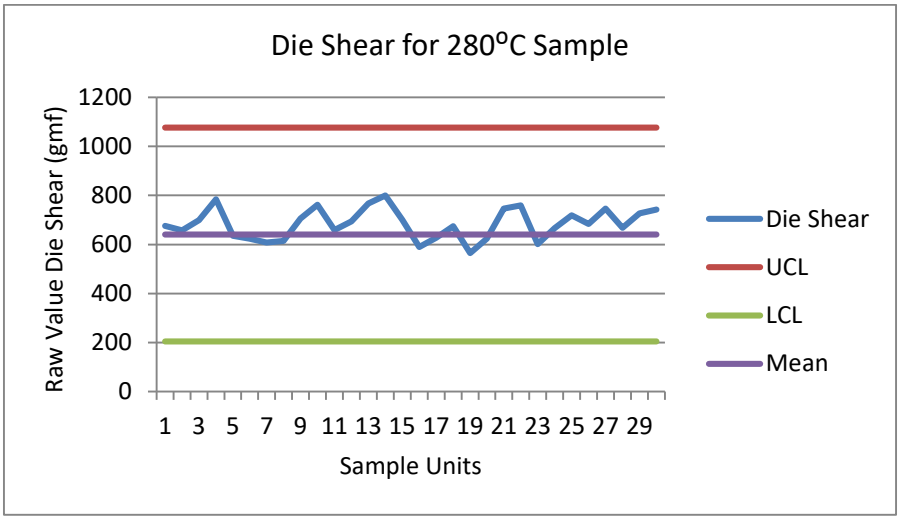


Fig. 15. Die shear test of 280 °C sample

Figure 16 shows the die shear test value versus bonded units at 290°C. A total of 30 samples of flip chip units were bonded at 290°C. From the Figure 16 it can be observed that the maximum die shear value is 874.9gmf and average value of die shear value is above 800gmf. Besides that, the minimum die shear value observed is 640.1gmf. Overall all the bonded units are above mean value and in range of the border of lower control limit (LCL) and upper control limit (UCL). This can be concluded that the higher the die shear value, the higher the strength of the units bonded on the surface of the copper pad. Based on Figure 15 and Figure 16, the die shear value of batches prepared at temperature of 290°C shows higher values compared to 280°C batches.

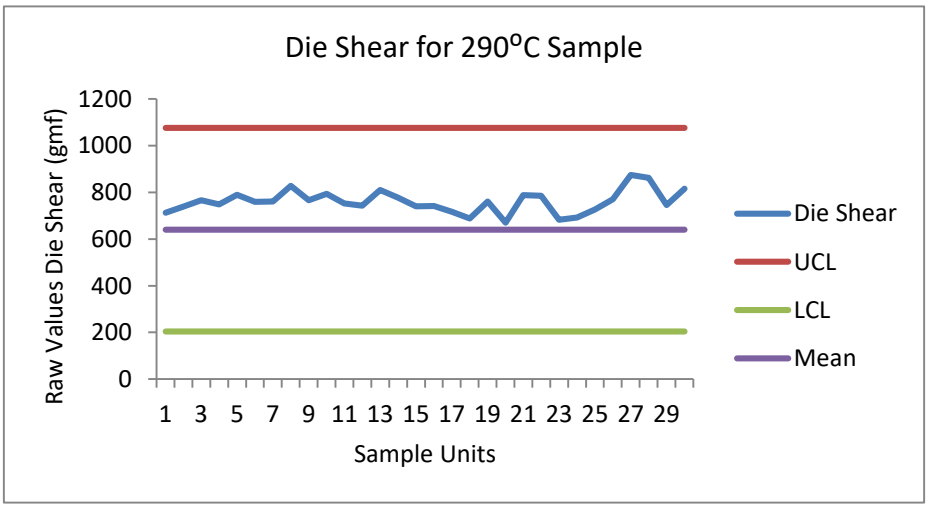
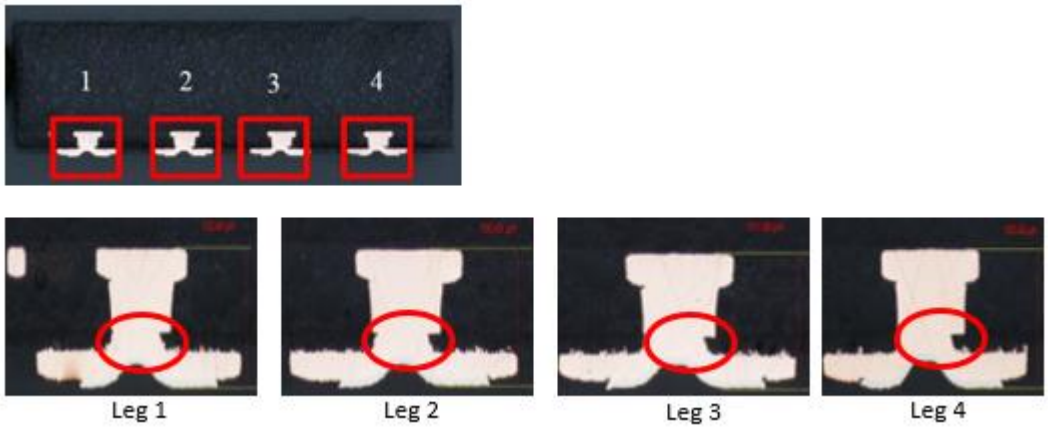
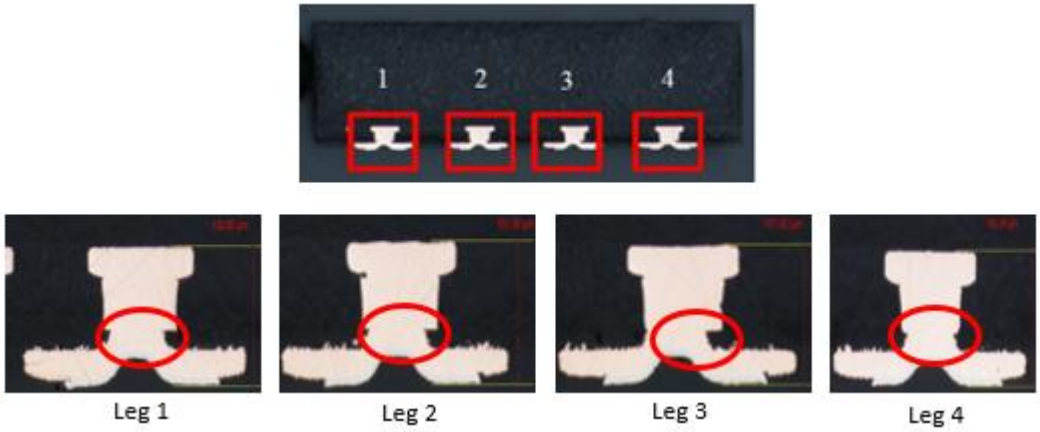


Fig. 16. Die shear test of 290°C sample

3.2 The Formation of Copper Pillar Solder in Cross Section Area Examination with Various Temperature Bonding

Table 6 shows the experiment results of samples that are prepared by using two types of temperature, which is at 280^{o}C and 290^{o}C soldering temperature. The samples are tested in the cross section area to observe the copper pillar leg solder.

Table 6
Cross Section Area of copper pillar solder after bonding

Temperature of Sample	Cross X-Section Area of Copper Pillar Solder
280 ^{o}C	
290 ^{o}C	

After cross section, Table 6 shows the image of copper pillar solder for four legs that has been prepared for cross section inspection with respect to samples prepared at both temperatures. For samples prepared at 280^{o}C, it can be observed that the copper pillar solder is thin at the interconnection of copper leg. As circled in red, the copper pillar interconnection can be seen to be fragile and the gap of pillar is not evenly. This will cause the of copper pillar interconnection to have crack issues. The crack may be occurring due to low melting condition of the copper. The thinner the copper pillar interconnection, the more cracks will be developed in the copper pillar. At 290^{o}C, it can be observed that the formation of copper pillar solder interconnection is thicker compared to the 280^{o}C copper pillar. The formation of solder joint interconnection between the copper pillar and the interconnection of leg as circled in red shows thick layer of copper pillar. At 290^{o}C setting, each leg interconnection of copper pillars is noted to be evenly melted and copper pillar thickness is comparable with 280^{o}C.

3.3 The Formation of Intermetallic Growth of Copper Pillar Solder with Various Temperature Respect to Staging Time

By conducting an experiment by using two groups of sample with soldering temperature at 280^{o}C and 290^{o}C, direct measurement of the intermetallic thickness can be used to reflect the intermetallic growth rate during soldering process condition by controlling the atmospheric environment condition. Based on the data taken from study, it is now clear that the temperature performs an important factor in determining the initial grow formation of both intermetallic species but at prolong duration of exposure, the growth rate start to slow down due to the resistance of Sn atom mobility to cross the intermetallic barrier as shown in Figure 17 and Figure 18.

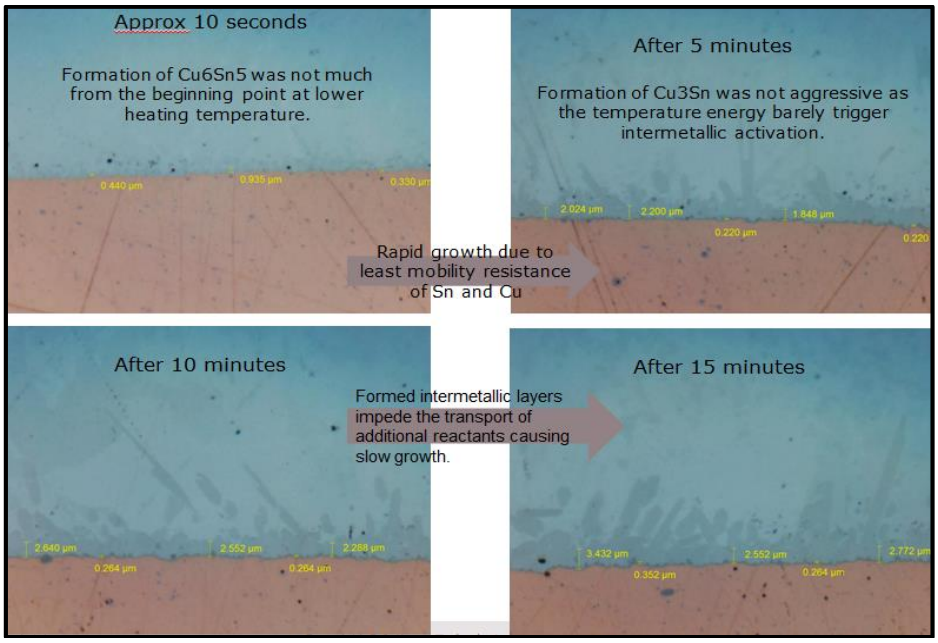


Fig. 17. Metallographic data from 280^{o}C soldering temperature respect to staging time

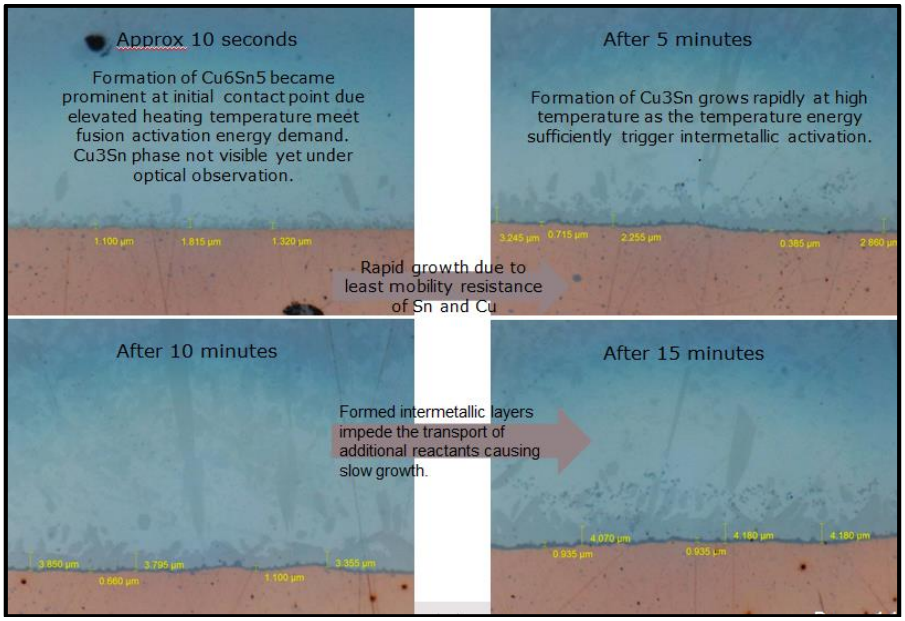


Fig. 18. Metallographic data from 290^{o}C soldering temperature respect to staging time

By studying the behaviour of 40 cross section samples under different atmospheric condition and soldering temperature, a graph was tabulated as to clearly show the interaction between the intermetallic thicknesses versus the temperature as shown in Figure 19. Approximation of parabolic growth curve, as expressed by Eq. (1).

$$X = \sqrt{(kt)} \quad (1)$$

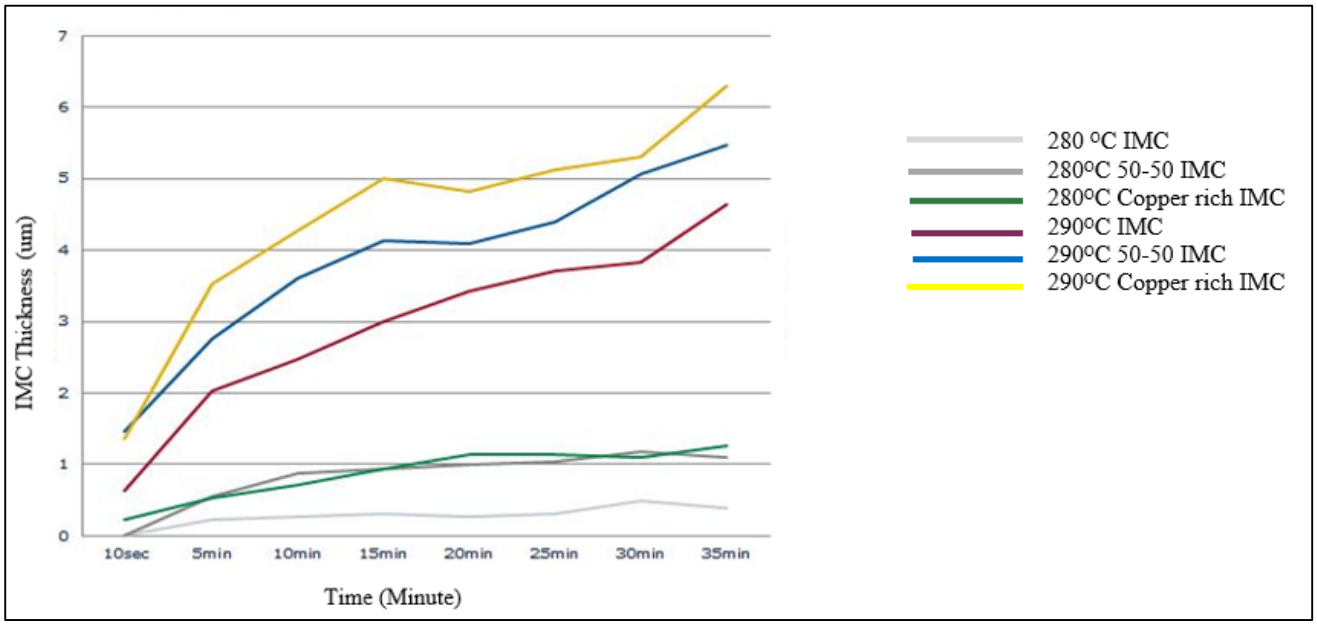


Fig. 19. Intermetallic growth versus staging time

4. Conclusions

All the experiments shown in this technical paper points out the validity of the fundemental study and these findings open up ways for process to have better guidance to control critical parameters for processes that deals with soldering process as to counter premature defects like intermetallic coverage, overheated temperature or long staging time of bonding process. Besides tackling on in process difficulties, the methodology used in this experiments can be used to gauge the reliability of a copper pillar solder interconnection in soldering process especialy for dealing with flip chip and non flip chip application. In conclusions, good copper pillar solder joint depends on the temperature parameter setting respect to staging time of flip chip bonding in order to ensure good interconnection of copper pillar connected to surface of the pad as well good intermetallic coverage. Thus, temperature play an important role to make sure the interconnection of copper pillar is strong and the behavior of intermetallic compound with respect to various temperature setting. In addition, various innovations are still in progress to make copper pillar technology more stable and more cost effective.

Acknowledgements
The author wish to express his thanks to the Ministry of Education and Universiti Teknikal Malaysia Melaka for the financial support using FRGS/1/2016/TK03/FKM-CARE-F00317.

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