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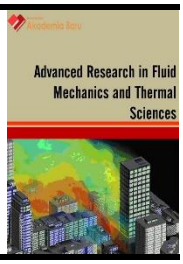

Thermal Impact of Heat Spreader Co-Planarity to Electronic Packaging

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ABSTRACT

This study presents the thermal impact of heat spreader co-planarity on the flip chip package with heat spreader. The co-planarity of heat spreader changes the thermal performance of the flip chip package significantly, especially the junction-to-case thermal resistance of the package. A numerical study using ANSYS Icepak was conducted to investigate the thermal degradation of heat spreader with concave and convex deflection up to 0.12 mm. The result indicates that the concave deflection causes improvement while convex deflection causes degradation in junction-to-case thermal resistance of the flip chip package. The outcome of the study recommends the co-planarity tolerance for the heat spreader shall not be greater than 0.07 mm for a 60 mm x 60 mm flip chip package with the dissipation power of 150 W.

1. Introduction

The thermal characterization data for the electronic package such as junction-to-ambient (Θ_{JA}), junction-to-board (Θ_{JB}) and junction-to-case (Θ_{JC}) thermal resistances are commonly found in any electronic packaging datasheet. Θ_{JA} value is essential to the end user during the heat sink selection [1] in the system design and to determine whether a natural convection or forced air convection cooling design is required. While Θ_{JB} and Θ_{JC} are crucial to the end user especially when the product designer wants to predict the maximum junction temperature (T_J) of the electronic package in the system using Computational Fluid Dynamics (CFD) simulation. Most of the CFD simulation tools allow packaging modelling simplification by using two resistance model or also known as 2R model without the need to build a detail packaging model in the simulation as presented by Shidore [2-4]. The 2R is defined in JESD15-3 [5] and the 2R refers to the Θ_{JB} and Θ_{JC} values provided in the package datasheet.

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Normally, thermal characterization analyses are carried out with the assumptions that all parts in the packaging are at nominal and perfect conditions. There is no co-planarity issue on all the parts of the flip chip package. The thermal interface material 1 (TIM1) as defined by Gowda [6] is assumed to fill up the gap between the silicon die and the heat spreader perfectly without any void. However, in reality, the warpage can be easily found on the heat spreader and it becomes even more severe when the package size is bigger with heat spreader of larger surface area. The co-planarity of the heat spreader creates voids on TIM1 material that eventually degrades the heat transfer from the silicon die to the heat spreader [7-9]. As a result, the junction-to-case thermal resistance increases significantly.

Typically, for a flip chip package with a heat spreader, Θ_{JC} in the range of 0.05 to 0.10 ^{o}C/W [10] depends on the design of the package. For a high power packaging, a small variation of Θ_{JC} value will cause a significant difference on T_J. For instance, a package with a dissipation power of 300 W with variation of 0.05 ^{o}C/W on Θ_{JC} will cause 15 ^{o}C difference on the junction temperature. Therefore, the accuracy of Θ_{JC} value is very important in order to prevent an overestimation or underestimation of the maximum junction temperature of the package that will eventually increase the product cost.

2. Thermal Analysis with Computational Fluid Dynamics (CFD) Approach

A 60 mm x 60 mm flip chip package with heat spreader of 1 mm in thickness and 150 W uniform power map is used as the test vehicle for the thermal characterization analysis. All the components are modelled in detail, except the substrate, solder bumps with underfill and solder balls are lumped models. The lumped models are assigned with estimated equivalent orthotropic thermal conductivities as summarized in Table 1. The 2s2p board is modelled according to JEDEC specification of JESD51-9 [11], modelled in detail with traces and metal layers imported from the board design file.

Table 1
Lumped Models summary

Lumped Model	Orthotropic Thermal Conductivity
Substrate	(47.2 7.6 47.2) W/m.K
Bump/Underfill	(0.966 20.319 0.966) W/m.K
Solder Ball	(0.05 18.48 0.05) W/m.K

The concave and convex deflections up to 0.12 mm are investigated under the heat spreader co-planarity study. The heat spreaders with concave and convex deflections are modelled separately as CAD geometries using Solidworks before being imported to ANSYS Icepak. The heat spreaders with concave and convex deflections are shown in Figure 1 and Figure 2 respectively.

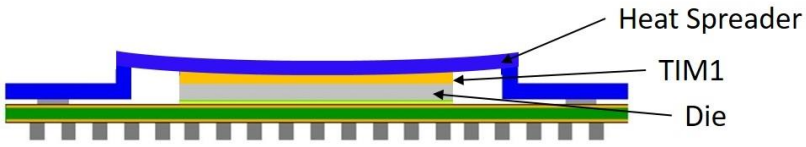

Fig. 1. Heat Spreader with Concave Deflection

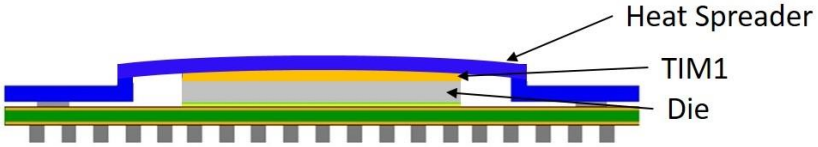

Fig. 2. Heat Spreader with Convex Deflection

Multiple non-conformal mesh assemblies are assigned in the model in order to generate sufficient tiny meshes to capture the deflection profile and slowly transition to coarser meshes to the JEDEC 2s2p board and then the test fixture. The meshes generated are shown in Figure 3.

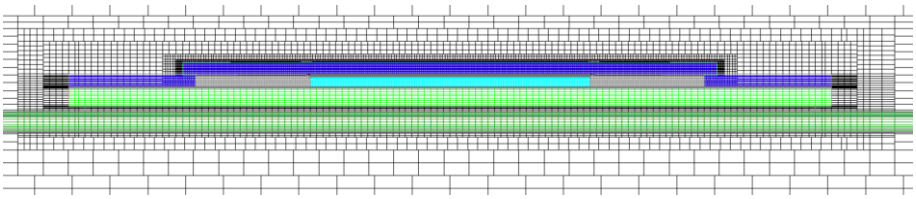

Fig. 3. Meshes of the Package and Board Assembly

2.1 Θ_{JA} Thermal Characterization Analysis

The simulation model for Θ_{JA} thermal characterization is constructed according to the standard test methodology that is defined by JC-15 Committee in JESD51-2 [12] and JESD51-2A [13] as shown in Figure 4. Θ_{JA} simulation runs at natural convection environment at ambient temperature of 25 ^{o}C until steady state is reached. The setup of this simulation can be summarized as Table 2.

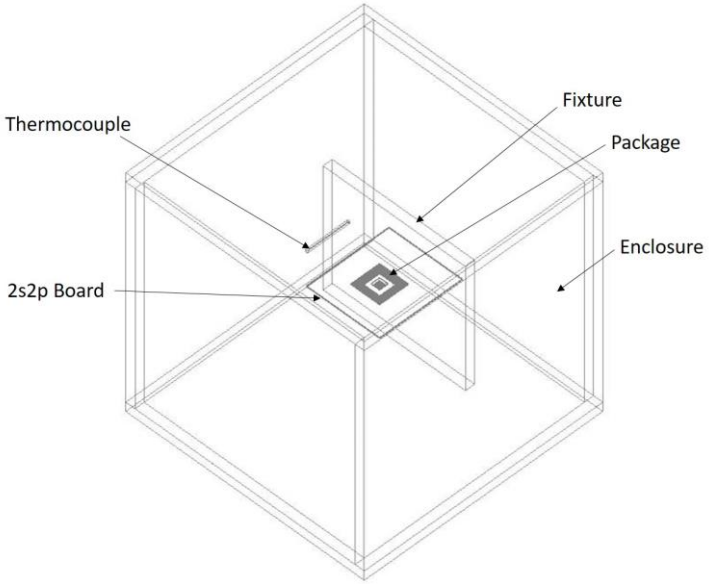

Fig. 4. Θ_{JA} Simulation Modelling

Table 2
θ_{JA} Simulation Setup summary

Simulation Setup	Mode
Flow	On
Temperature	On
Radiation	On
Gravity	On
Flow Regime	Turbulent – Zero Equation

Θ_{JA} under these conditions can be determined from Eq. (1) below [12,13].

$$\theta_{JA} = \frac{T_J - T_A}{P_H} \quad (1)$$

where the T_J is junction temperature of the device at steady state, T_A is the ambient temperature and P_H is the power dissipation of the device respectively.

2.2 Θ_{JB} Thermal Characterization Analysis

The Θ_{JB} simulation model is constructed based on the JEDEC standard, defined in JESD51-8 [14] as shown in Figure 5. The ring style cold plates as defined in JEDEC are simplified by removing the water channels from the cold plates. The water channels are being replaced by applying constant temperature wall boundary conditions around the exterior surfaces of the top and bottom cold plates to mimic the constant temperature from the water cooling effect. Therefore, the junction-to-board thermal characterization is simulated under pure conduction heat transfer until steady state is reached with the simulation setup as summarized in Table 3.

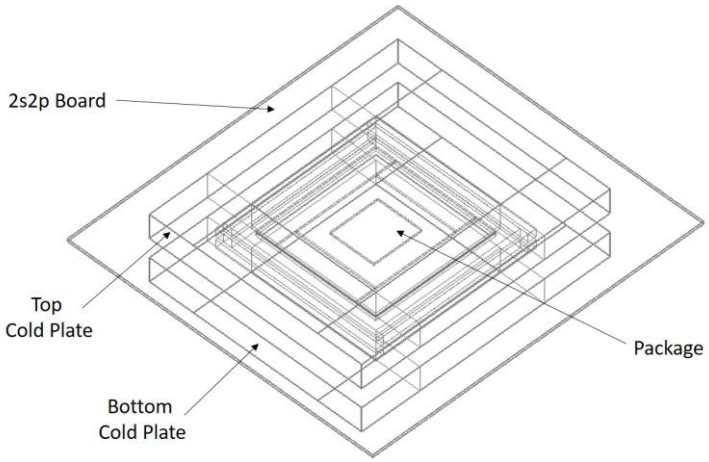

Fig. 5. Θ_{JB} Simulation Modeling

Table 3
θ_{JB} and θ_{Jc} Simulation Setup summary

Simulation Setup	Mode
Flow	Off
Temperature	On
Radiation	Off
Gravity	Off
Flow Regime	N/A

Θ_{JB} under these conditions can be determined from Eq. (2) below [14].

$$\Theta_{JB} = \frac{T_J - T_B}{P_H} \tag{2}$$

where the T_J is the junction temperature of the device at steady state, T_B is the board temperature and P_H is the power dissipation of the device respectively.

2.3 Θ_{JC} Thermal Characterization Analysis

Similar to Θ_{JB} simulation model, the Θ_{JC} simulation model is constructed based on the test setup used in DELPHI compact model project as shown in Figure 6. The water channels of the cold plates are removed and replaced by constant temperature wall boundary conditions around the top and

bottom cold plates exterior surfaces to mimic the constant temperature from the water cooling effect. The TIM2 material is applied between the package and the top cold plate. The TIM2 material's parameters are summarized in Table 4. Θ_{JC} characterization is simulated under pure conduction heat transfer until steady state is reached with the simulation setup similar to Θ_{JB} simulation shown in Table 3.

Table 4
TIM2 Material summary

TIM2 Material Parameter	Value
Bond Line Thickness	0.26 mm
Thermal Conductivity	2.3 W/m.K

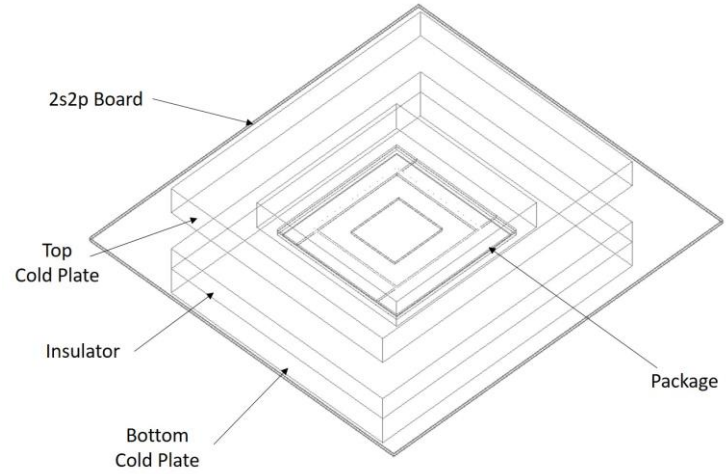

Fig. 6. Θ_{JC} Simulation Modeling

Θ_{JC} under this condition can be determined from Eq. (3) below.

$$\Theta_{JC} = \frac{T_J - T_C}{P_H} \tag{3}$$

where the T_J is the junction temperature of the device at steady state, T_C is the case temperature and P_H is the power dissipation of the device respectively.

3. Results

Several simulations are carried out to investigate the thermal impact of heat spreaders with concave and convex deflections up to 0.12 mm in the flip chip package. The thermal resistances in the graphs shown in this section are based on calculations of the simulated temperatures obtained from the simulations using Eq. (1)-(3).

3.1 Θ_{JA} Thermal Characterization Result

The temperature and airflow distribution patterns for this simulation are shown in Figure 7, respectively. Figure 8 shows Θ_{JA} simulation results for convex and concave deflections from 0 to 0.12 mm. Results show that Θ_{JA} improved by concave deflection while degraded by convex deflection. Nevertheless, the improvement and degradation are less than 1% if comparing both Θ_{JA} at 0.12 mm

deflection to zero deflection. 1% of degradation equals to rise in junction temperate by 5 ^{o}C in the package with a dissipation power of 150 W.

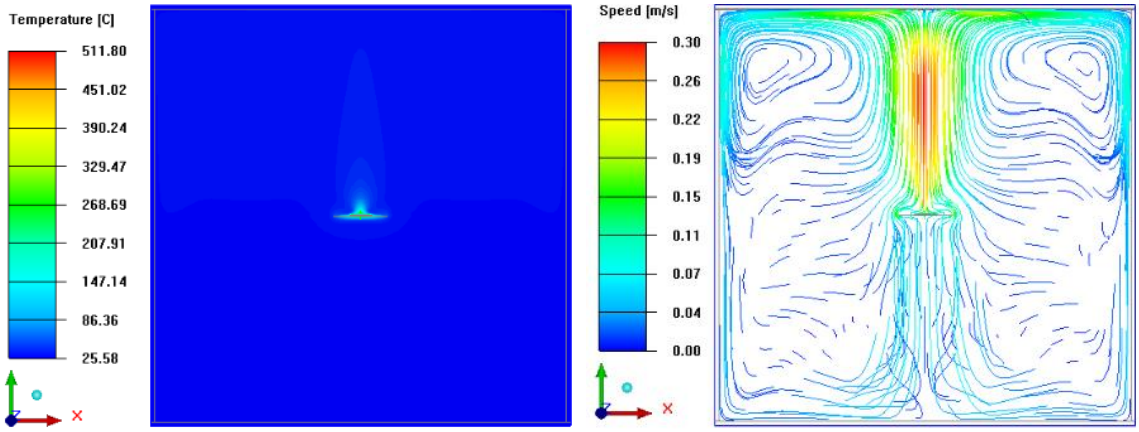

Fig. 7. Θ_{JA} Simulation Temperature Distribution (right) and Airflow Pattern (left)

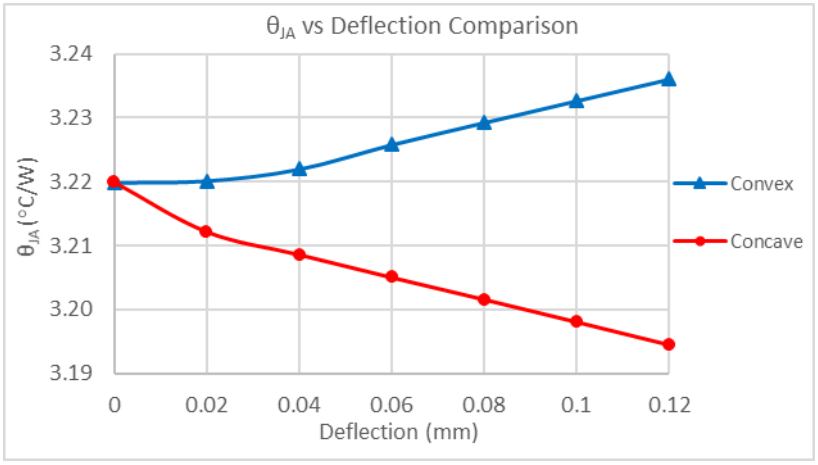

Fig. 8. Θ_{JA} vs Deflection Simulation Data Comparison

3.2 Θ_{JB} Thermal Characterization Result

The temperature distribution of the package and board assembly for Θ_{JB} simulation is shown in Figure 9. Θ_{JB} simulation results show the similar trends as Θ_{JA} as shown in Figure 10. Both convex and concave deflections cause variation of less than 1% if comparing Θ_{JB} at 0.12 mm deflection to zero deflection. 1% variation of Θ_{JB} equals to 5 ^{o}C variation of junction temperature in the package with a dissipation power of 150 W.

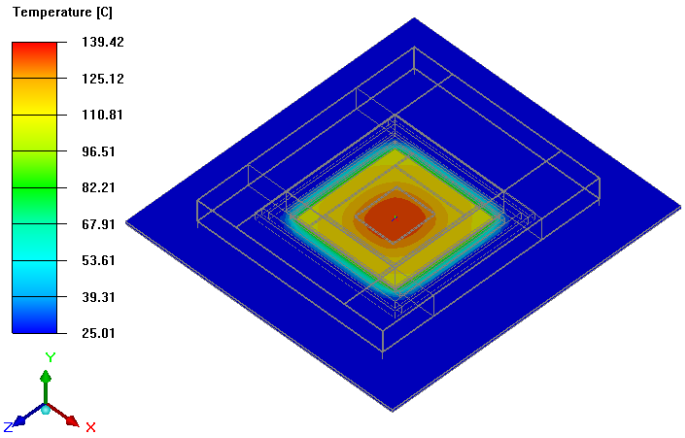

Fig. 9. Θ_{JB} Simulation Board with Package Temperature Distribution

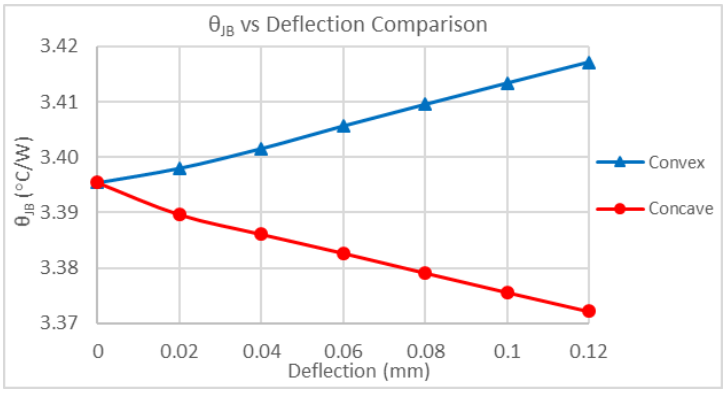

Fig. 10. Θ_{JB} vs Deflection Simulation Data Comparison

3.3 Θ_{JC} Thermal Characterization Result

The temperature distribution for Θ_{JC} simulation is shown in Figure 11. The convex deflection causes significant degradation while concave deflection improves the Θ_{JC} of the flip chip package according to the simulation results as shown in Figure 12. If the targeted degradation is less than 5 ^{o}C of variation in junction temperature, junction-to-case thermal resistance must not be greater than 0.105 ^{o}C/W which leads to deflection of 0.07 mm referring to chart in Figure 12.

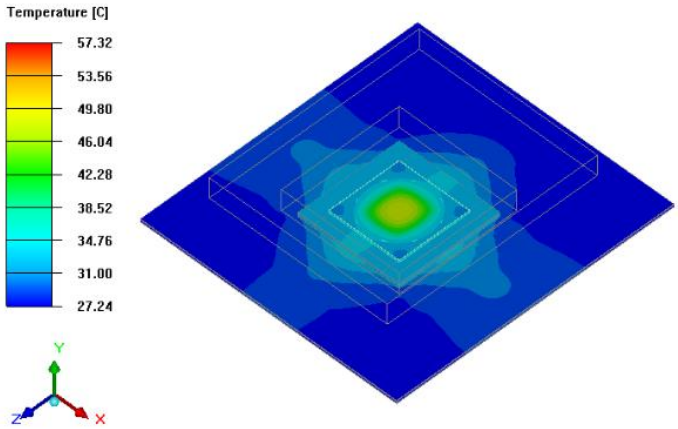

Fig. 11. Θ_{JC} Simulation Board with Package Temperature Distribution

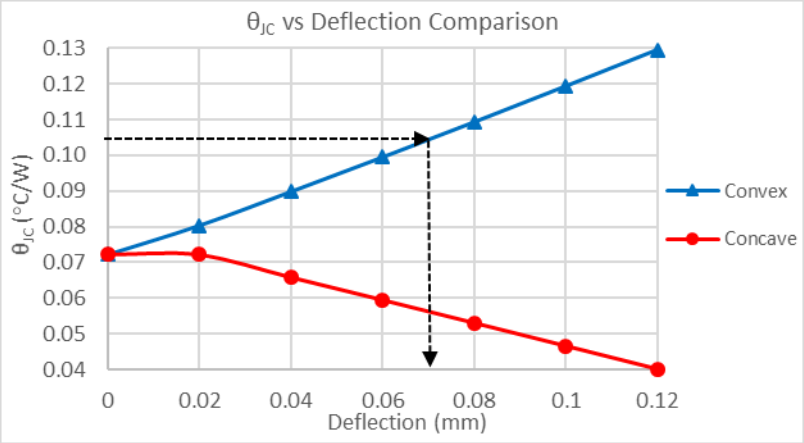

Fig. 12. Θ_{JC} vs Deflection Simulation Data Comparison

The concave profile reduces the BLT while the convex profile increases the BLT of the TIM1 material in the flip chip package. According to Fourier's Law of heat transfer [15], the rate of heat conduction is inversely proportional to the thickness of medium, which is the BLT of TIM1 material in this case. Therefore, the results are compliance to Fourier's Law.

4. Conclusions

It can be concluded that both the concave and convex deflections up to 0.12 mm on the heat spreaders do not cause significant degradations to the Θ_{JA} and Θ_{JB} of the flip chip package. However, the deflections on the heat spreader change the Θ_{JC} significantly. Θ_{JC} is approximately doubled if comparing the Θ_{JC} at 0.12 mm convex deflection to zero deflection. In order to not exceed 5 ^{o}C increase of the junction temperature due to the deflection of the heat spreader, acceptable co-planarity tolerance of the heat spreader should not be greater than 0.07 mm for a 60 mm x 60 mm flip chip package with 150 W dissipation power.

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