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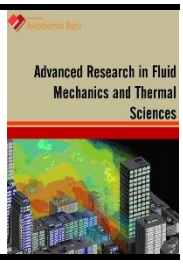

Heat Transfer Analysis of Diffusion Furnace for Wafer Annealing Process

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ABSTRACT

Diffusion furnaces in semiconductor manufacturing processes are used to grow oxide on silicon wafer surfaces or diffuse dopants into semiconductor wafers. During such process, the silicon wafers are heated in furnaces to temperatures typically in the range between 973K to 1523K. In this study, a two-dimensional axisymmetric model is employed to simulate the vertical furnace that operates at temperature 1123K. The simulation results on profile temperature distribution of a baseline case having 175 silicon wafers with diameter size of 200mm in a process tube are in good agreement with that of experimental data. The experimental data gained from furnace which was heated at 1123K is employed as a benchmark for this numerical assessment. It is also shown that uniform heating can be applied on the bulk region of the stacked wafers. In this study, the influences of heater temperature and the gap between wafers arranged in the process tube on temperature field in the process tube have been explored. From the simulations, it is worth highlighting that the temperature distribution over the bulk region of the stacked wafers is in accordance with heater temperature. In addition to that, it is found that annealing process over lesser number of wafers (with larger wafer gaps) in the boat may not significantly affects the heating performance in the furnace.

1. Introduction

There are two types of semiconductor furnace orientations available in the market, which are horizontal type and vertical type furnaces. Initial designs for semiconductor diffusion processing furnaces were configured with the wafer array and processing chamber arranged in a horizontal orientation, which was patented by Reynolds and Holloway in 1965 [1]. However, there are complications occurred arising from conventional horizontal furnaces including wafer-to-wafer

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thickness uniformity degradation and thicker native oxides due to the quantity of air allowed during loading. Campbell and Miller in 1982 have patented a vertical oriented furnace to run chemical deposition (CVD) process [2]. The invention of chemical deposition was processed in a controlled temperature reaction zone having a temperature from 523K to 1573K. Apart from horizontal type furnace, furnaces with vertically arranged wafer arrays and processing chambers were designed in the attempt to provide better control of temperature. As compared to horizontal type furnace, the vertical type furnace provides a space saving advantage as compared to horizontal furnace. As expected, the vertical configuration furnaces are now commonly used by most of semiconductor wafer fabrication manufacturers.

Flow and heat transfer studies on diffusion furnaces have been performed in many existing studies. Badgwell *et al.,* [3] measured wafer temperature in a multiwafer low pressure chemical vapor deposition (LPCVD). Coronell and Jensen [4] provided an alternative approach based on a direct simulation Monte Carlo technique to simulate the radiation heat transfer in a multi wafer LPCVD reactor. Hu [5] proposed a model to describe the transient temperature profile of wafers in a furnace during cooling. In this study, the convective heat transfer is deemed not significant and thus ignored for wafer cooling. Van Schravendijk *et al.,* [6] developed a method to estimate and control wafer temperatures in a horizontal type diffusion furnace. The heat transfer model considers energy balances for the insulation, reactor doors, heating coils, process tube, and wafers. Tavel and Hearn [7] developed a model to estimate the maximum temperature difference across a wafer during furnace processing. Radiation between the end wafers and the reactor doors was neglected. The paper concludes the highest radiant thermal stress occurs during the unload sequence, and that the thermal stress can be reduced by unloading the wafers slowly. A simplified heat transfer model was used by Ko *et al.,* [8] to predict the water temperature distribution in the vertical furnace. Apart from diffusion furnace, thermal modelling has been vastly studied in other furnaces, for example in pyrolysis gas furnace [9].

There are many factors that could affects the Silicon wafer during annealing process. The influence of temperature distribution in the vertical furnace on thickness uniformity of the silicon film have also been documented by Yang *et al.,* [10]. As highlighted in the many existing studies, the contributing factors can be the wafer sizing [11], gas flow behavior [12], flow rate [13], thermal insulation structure [14], furnace orientation [15] and window thermal diffusivity [16]. This study intends to further investigate the influences of heater temperature and wafer spacing gaps on the heating uniformity over the stacked wafers in a vertical oriented furnace.

2. Methodology

A typical furnace used in semiconductor manufacturing process consists of an open elongated process tube surrounded by heating element, as depicted in Figure 1. The heating elements usually comprised of stainless steel while the inner layers of insulating component are made of ceramic fiber. Inside the heater element, there are helical resistance coil which is made of chrome-aluminum-iron alloy surrounding the quartz tube. The process tube which is made from quartz is designed with one end allowing input gasses to enter while the other end is open to discharge the scavenger exhaust process gas and by-product. Silicon wafers generally placed on the carrier known as quartz boat that is placed in the tube during loading. The quartz boats with the arranged wafers, is pushed into the hot zone of the furnace where the wafers are heated for a certain amount of time in a single process cycle. A full annealing cycle consists of

I. pre-loading of the wafers into the quartz boat;
II. positioning of the loaded quartz boat into the furnace using a robot;
III. execution of the annealing cycle;
IV. furnace cool-down followed by removal of the quartz boat from the furnace;
V. unloading of the annealed wafers from the quartz boat.

The functions of quartz assembly components in furnace are summarized in Table 1. The studies of current research are focused on the annealing process which running at 5 zone vertical furnace at the temperature of 1123K. Conventionally, there were 175 wafers were arranged vertically filling up the entire quartz boat. The wafers are then heated in the chamber filled with nitrogen gas.

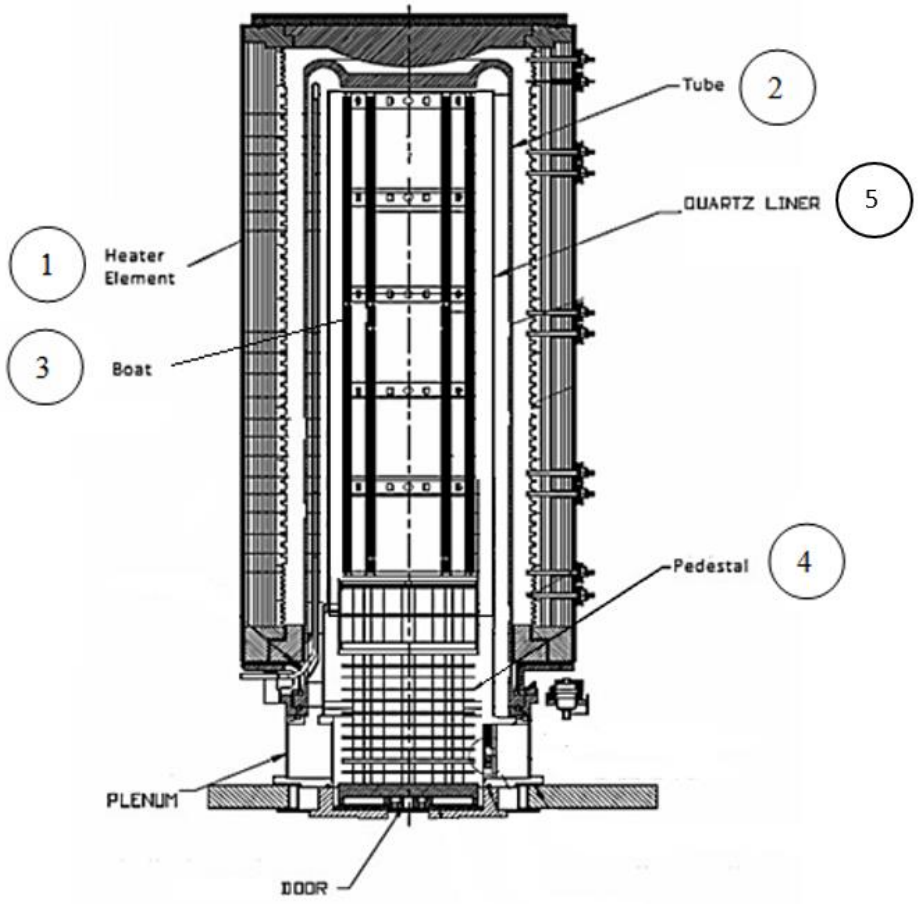


Fig. 1. Cross section of vertical type furnace

Table 1
The functions of quartz assembly components in furnace

Location	Component of LHP	Function
1	Heater element	The unit consists of high resistance heating coils to produce heat provided to process tube when power is supplied
2	Process Tube	Enclosed chamber to deliver process gas to semiconductor wafers and perform diffusion process at specific high temperature
3	Boat	A carrier to place semiconductor wafers in process tube to conduct diffusion process
4	Pedestal	The pedestal place under the quartz boat carrier is loaded into the process chamber through the load door at the bottom of chamber.
5	Liner	An inner wall located inside process tube to direct the process gas flow through to the entire wafer stack from top to bottom uniformly

3. Assumptions

Figure 2 depicts the schematic diagram of a diffusion furnace. The furnace contains 5 zones of heater element around the heater wall of the furnace. The Zone 1 of the heater is located at top region of the furnace while Zone 5 is located at the bottom region of the furnace. For this study, a few assumptions have been made, as stated below

i. The is no heat loss through the tube from the torch to the tube inlet.
ii. The effects of quartz boat carrier are neglected.
iii. The variation of the flow and temperature with respect to azimuthal direction are neglected.
iv. The gaps between the heater and the process tube is neglected.

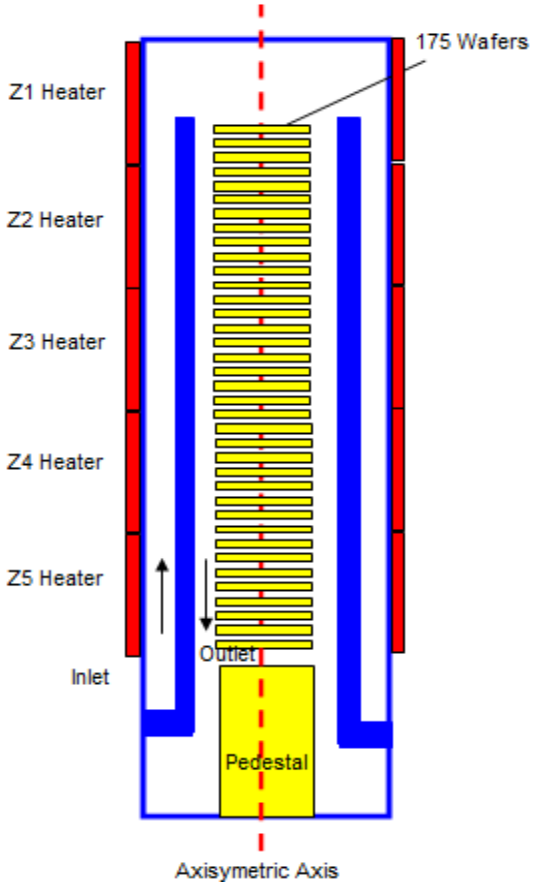


Fig. 2. Schematic of vertical type furnace

4. Methodology

In this study, steady laminar flow passing through the furnace is considered. Based on the experimental work, the flow is of low Reynolds number. Using hydraulic diameter ($D_h = D_o - D_i = 0.024\text{m}$) as the characteristic length, the flow rate of $0.5\,\text{l/min}$ yields $Re_{D_h} = 0.1321$. The outer diameter and inner diameter are represented by D_o and D_i, respectively. The governing equations are thus given by

Continuity: $\nabla \cdot \vec{V} = 0$ (1)

Momentum: $\nabla \cdot \left(\vec{V}\vec{V}\right) = -\nabla p + \nabla \cdot (\bar{\bar{\tau}})$ (2)

Energy: $\nabla \cdot \left(\rho \vec{V} E\right) = \nabla \cdot (k \nabla T)$ (3)

where $\vec{V}$ is the velocity vector and p is the static pressure. The stress tensor is denoted by $\bar{\bar{\tau}}$. Energy per unit mass and temperature are represented by E and T, respectively. Meanwhile, ρ is the density. In this study, viscous heating is not considered. Uniform flow velocity is imposed at the inlet and zero static pressure is prescribed at the outlet. Heat flux is imposed on the top and bottom covers. Along the heater walls, combined convection and radiation boundary conditions are employed. The heat flux imposed on the walls are given by

$$q = h_f\left(T_w - T_f\right) + \epsilon\sigma(T_\infty^4 - T_w^4) \quad (4)$$

where h_f is the heat transfer coefficient, ϵ is the emissivity of the wall, and σ is the Stefan-Boltzmann constant ($5.67 \times 10^{-8}\mathrm{Wm^{-2}K^{-4}}$). In this study, the emissivity of the heater wall is taken to be 0.85. Wall temperature, fluid temperature and temperature of surrounding surface are denoted by T_w, T_f and T_∞, respectively. At $1123\mathrm{K}$, the density and the dynamic viscosity of nitrogen are $0.3005\ \mathrm{kg/m^3}$ and $44.88 \times 10^{-6}\mathrm{Pa.\,s}$, respectively. The heat capacity c_p and heat conductivity k of nitrogen, quartz and wafer as stated in Table 2.

Table 2
Heat capacity and heat conductivity

	Heat Capacity c_p $[\mathrm{J/kg.\,K}]$	Heat Conductivity k $[\mathrm{W/m.\,K}]$
Nitrogen	1191	0.07215
Quartz	740	1.38
Wafer	780	330

Since the furnace is of cylindrical shape, the flow and temperature fields are mainly dependent on axial and radial directions, the variations in the azimuthal direction are thus neglected. This permits the use of two-dimensional axisymmetric model (as depicted in Figure 3) to simulate the heat transfer in the vertical furnace. The furnace domain considered in this study is of the length of $1.13\mathrm{m}$ long and $0.14\mathrm{m}$ radius. All five of the heater walls has equal length of $0.226\mathrm{m}$. The quartz liner is of $0.006\mathrm{m}$ thickness and $1.042\mathrm{m}$ length. The flow passage between quartz liner and heater wall is $0.0012\mathrm{m}$. Uniform structured grid with fine resolution of $N_z \times N_r = 1130 \times 140$ is employed in this study.

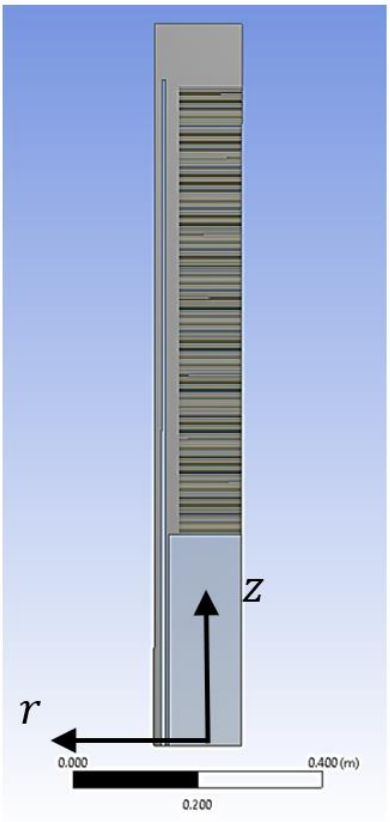
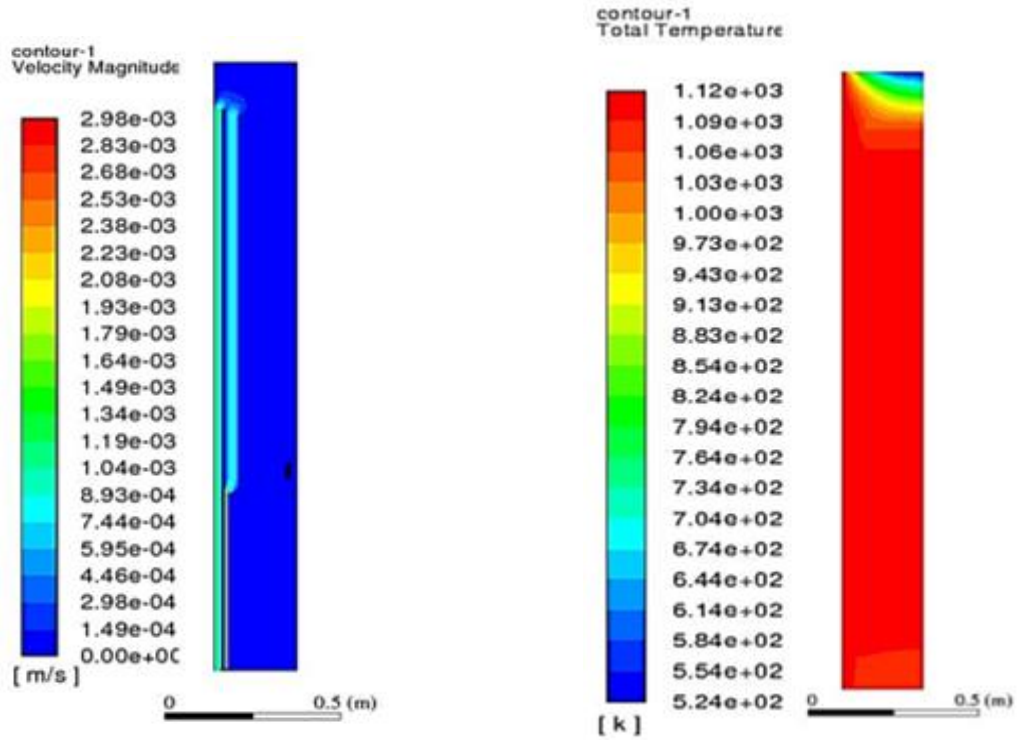


Fig. 3. Two-dimensional axisymmetric computational domain for furnace with 175 wafers

5. Results and Discussion

A baseline simulation is performed according to the experimental work done and the simulations were conducted using ANSYS Fluent. The experimental data gained from furnace which was heated at $1123\mathrm{K}$ is employed as a benchmark for this numerical assessment. Nitrogen is allowed to flow from torch through tube inlet at the temperature of $1073\mathrm{K}$ at the flow rate of $0.5\ \mathrm{l/min}$ toward a 175 pieces of stacked Silicon wafers of $200\ \mathrm{mm}$ diameter, and then flow past quartz pedestal until the exhaust outlet of the tube in order to ensure no oxygen in the chamber. The gap between each stacked wafer, also referred as wafer-to-wafer vertical spacing is $3\mathrm{mm}$. The annealing process will treat the wafer surface at the temperature of $1123\mathrm{K}$ inside the chamber filled with nitrogen gas. Heat flux of $200\mathrm{W/mK}$ through both top and bottom covers are prescribed in the simulation, arising from the significant heat lost noticed from both covers to the ambient in the experimental work. The velocity field and temperature field of the baseline case are illustrated in Figure 4(a) and Figure 4(b), respectively. As can be observed from Figure 4(a), the nitrogen gas flows along the narrow passage between heater wall and quartz liner from the inlet at the bottom and rise to the region above the quartz liner, the nitrogen gas will then descends downward passing through the passage between stacked wafers and quartz liner. It is also worth to highlight that that flow between narrow gap between stacked wafers is minimal. As expected, based on the temperature field, lower temperature is attained at both the upper and lower region of the furnace. This is due to the heat lost through the top and bottom covers of the furnace. At the lower region, the presence of pedestal prevented the

temperature field to reduce significantly. In contrast, the upper region is directly exposed to the top cover, this give rise to a substantially lower temperature in that region, as visible in Figure 4(b).



(a) (b)

Fig. 4. (a) Velocity field and (b) temperature field for baseline case

Based on the temperature field obtained from the baseline case, the profile temperature distribution attained are then compared to that of experimental data. The profile temperature distribution is obtained along the axial line at $r = 0.1195\text{m}$. It should be noted that the experimental temperature on each zone was measured in the steady state condition during annealing process. The experimental work was performed with the prescribed flow and heater temperature conditions using the vertical type furnace. As depicted in Figure 5, both experimental and simulation results are in good agreement with maximum error of 0.6%. It is also worth to mentioned that grid independence study is also carried out with finer grid resolution. Doubling the grid resolution in the radial direction to $N_z \times N_r = 1130 \times 280$ yield deviation at maximum of 0.03% as compared to the results obtained using $N_z \times N_r = 1130 \times 140$.

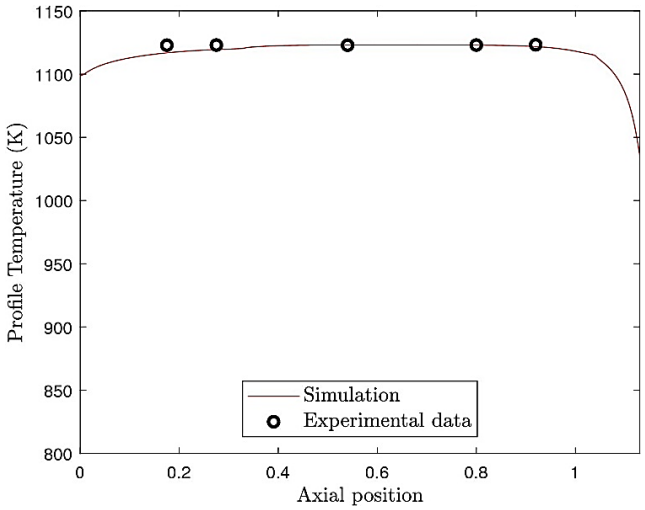


Fig. 5. Validation for profile temperature between experiments data and simulation results

5.1 Effects of Different Furnace Heater Temperatures

Figure 6 illustrates the stacked wafer centerline temperature for heater temperature fixed at 1123K, 1223K, 1323K and 1423K. This stacked wafer centerline temperature distribution is attained along an axial line from the center of the bottom wafer, $(r, z) = (0, 0.334)$, to the center of the top wafer, $(r, z) = (0,1.031)$. As expected, when a higher heater temperature is employed, a higher centerline wafer temperature distribution is attained. It is visible that the temperature profile along the wafer centerline exhibits similar trend where the temperature profile shifted upward when higher heater temperature is employed. At the bulk region of the stacked wafers, the temperature on the wafer is consistently heated at desired temperature, similar to that of furnace heater temperature.

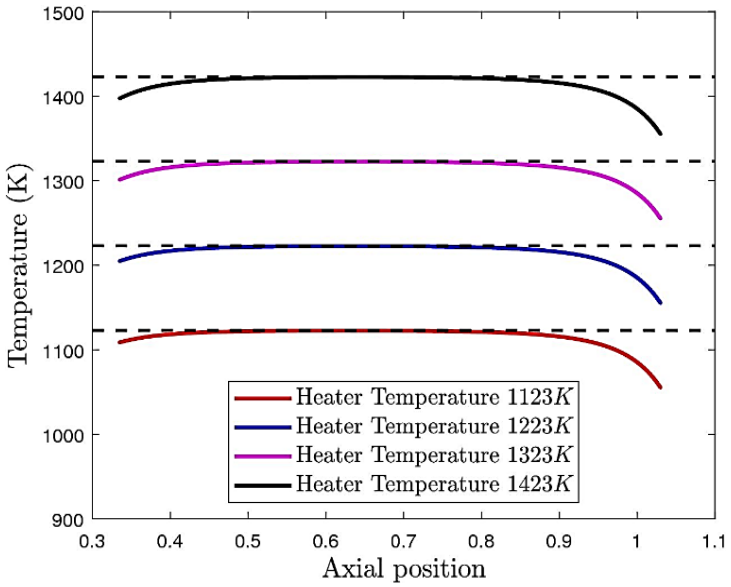


Fig. 6. Variation of furnace heater temperature along stacked wafer centerline at $1123K, 1223K, 1323K$ and $1423K$

As illustrated in Figure 7, the temperature distribution along radial direction (for wafer at the middle region of the stacked wafers) shows uniform heating across the wafer surface. In other words, there is no large radial temperature gradient on the wafer in the bulk region. This infers that the stacked wafers in the middle regions can be treated at the desired temperature. However, for all the heater temperatures investigated, as compared to the desired temperature (denoted by dashed lines), it is noted that the temperature at both upper and lower regions of the stacked wafers is slightly lowered. The reduced temperature at both upper and lower regions of the furnace would cause degradation to the wafer during annealing process. In this regions, dummy wafers are practically used instead.

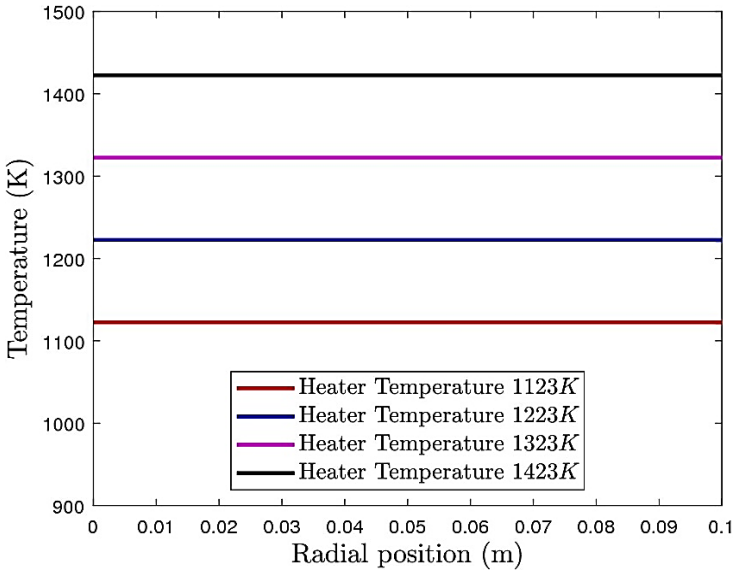


Fig. 7. Temperature distribution on wafer surface along radial direction for different heater temperature

5.2 Effects of Different Wafer Spacing

Apart from having different heater temperature, this study also examines the influences of the number of wafers stacked in the quartz boat on the temperature distribution. Figure 8 shows the temperature distribution for heating case with different wafer spacing, i.e., 3 mm, 4 mm and 5 mm. The total number of wafers in the quartz boat considered is 140 wafers and 115 wafers for 4 mm and 5 mm wafer spacing, respectively. As can be deduced from Figure 8, changing the wafer gaps may not affect the temperature distributions over the stacked wafers significantly. However, slight differences are noticeable on wafers in the proximity of top cover where reduced temperature is attained in this region when higher wafer spacing is employed. Despite the small differences, the result presented in Figure 8 may suggest that, in general, annealing process may not be affected by having quartz boat that contain lesser wafers.

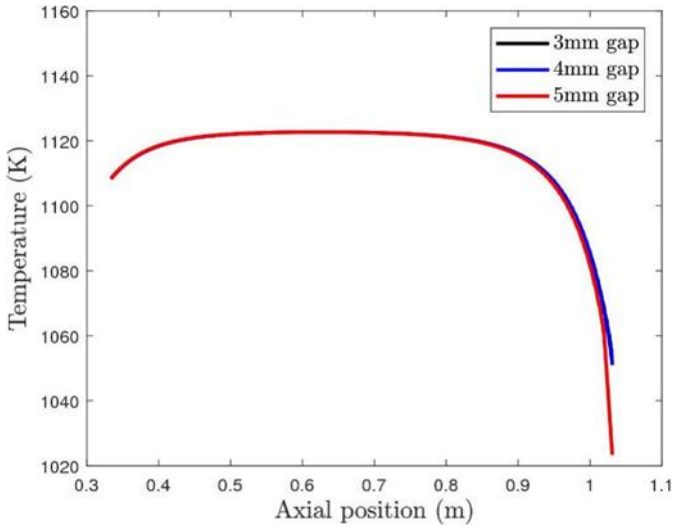


Fig. 8. The temperature distribution along the wafer centerline for different wafer spacings, i.e., 3 mm, 4 mm and 5mm

6. Conclusion

Heat transfer during annealing process in vertical furnace has been simulated in this study using two-dimensional axisymmetric model. This study examines the influence of different heater temperatures and different wafer spacing. It is shown that the heating is uniform over the entire region of stacked wafers, except in the upper and lower region, arising from the heat loss from top and lower covers. A similar trend of temperature distribution is obtained when higher heater temperature is employed. In addition, it is also shown that annealing process can be carried out on quartz boat without full capacity of wafers, without significantly degrading the heating over wafers.

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