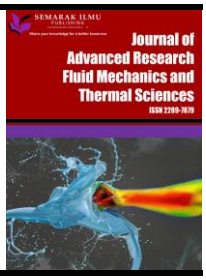
SEMARAK ILMU PUBLISHING

Journal of Advanced Research in Fluid Mechanics and Thermal Sciences

Journal homepage:
https://semarakilmu.com.my/journals/index.php/fluid_mechanics_thermal_sciences/index
ISSN: 2289-7879



A Review of Moldflow and Finite Element Analysis Simulation of Chip Scale Packaging (CSP) for Light Emitting Diode (LED)

Law Ruen Ching[1,*], Mohd Zulkifly Abdullah[2]

[1] School of Mechanical Engineering, Engineering Campus, Universiti Sains Malaysia, 14300 Nibong Tebal, Malaysia
[2] School of Aerospace Engineering, Engineering Campus, Universiti Sains Malaysia, 14300 Nibong Tebal, Malaysia

ARTICLE INFO

Article history:
Received 10 April 2022
Received in revised form 28 July 2022
Accepted 8 August 2022
Available online 5 September 2022

Keywords:
Chip scale packaging; light emitting diode; computer aided engineering

ABSTRACT

LED technology has been evolving aggressively in recent years from incandescent bulb during older days to as small as chip scale package. There is tremendous pressure to stay competitive in the market by optimizing products to next level of performance and reliability with shortest time to market. This changes the conventional way of product design and development to virtual prototyping by means of Computer Aided Engineering (CAE). The objective of the paper is to review challenges in chip scale packaging application in LED technology. The first part of the paper covered the literature survey of Chip Scale Packaging (CSP) in Light Emitting Diodes (LED), CSP architecture challenges, molding process and material for CSP. The findings of literature found that very few researchers had study silicone encapsulations process in CSP for LED in term of material characterization, mold process and simulation. Findings also shows that deployment Computational Fluid Dynamic (CFD) and integration of virtual prototyping using Finite Element Analysis (FEA) in product development in CSP for semiconductor industry had greatly reduced the time to market. However, there are very few papers discuss the application for CSP technology in LED industry. Second objective of the papers is discussion of methodolology in molding material characterization and simulation methodology. CFD helps to simulate the flow pattern of molding material as a function of different temperature, molding parameters settings for voids and displacement. FEA also help to evaluate the deformation of silicone in panel form and enable designer to predict the displacement of devices with different silicone.

1. Introduction

1.1 Chip Scale Packaging Challenges

In 2000s, when the revolution happened from conventional electronic packaging to Wafer Level-Chip Scale Packaging (WL-CSP), the whole industry needed a paradigm shift in assembly packaging process infrastructure. WL-CSP is attractive due to it cost per units, elimination of substrate and process simplification. Different type of technologies had been reviewed such as initial redistribution process by Fujitsu, Oki, FCT, Unitive and IZM-Berlin [1-4]. Tessera and Amkor technologies attach a

* *Corresponding author.*
E-mail address: rclawmy@yahoo.com

https://doi.org/10.37934/arfmts.99.1.158173

film to the wafer to create rerouting. [5-6]. Industry used nearly 2 decades to industrialized this technology by overcoming various issues in manufacturing and reliability of WLCSP technologies.

Solder joint reliability is one of the major issues in WLCSP technologies. Fan *et al.,* [7] presented that due to the thermal mismatch of thermal coefficient of thermal expansion (CTE) of silicon chip and the PCB material, solder balls became the weakest point of fan-out WLCSP technologies during temperature cycling. Fan *et al.,* [7] proposed to change the solder ball material and improve the CSP flexibility to reduce the stress at solder balls. Rogers *et al.,* [8] suggested fully molded Fan out WLP package mainly to eliminate active area of die edge exposure and Adaptive Patterning to compensate the die offset due to shrinkage of mold compound. This method proven to improve solder joint reliability even for big packages. As the WLCSP evolved into multi dies with complex interconnection and increase functionality, the packages became larger. Che [9] studied board level solder joint reliability for fan-out wafer level packaging for 15mm x 15mm and 20mm x 20mm packages. The paper concluded that the low CTE underfill and thin packages improve solder joint reliability. Mold compound played important role in determining solder joint reliability at package corner.

Warpage of the wafer is one of the major concerns in this technology. Kripesh *et al.,* [10] presented development for multi-die embedded wafer level packaging. The paper proposed the low CTE material compound and molding process optimization is important to reduce wafer warpage. Low temperature redistribution dielectric had been suggested to improve reliability of this technology. Che *et al.,* [11] conducted comprehensive study to reduce warpage of 12" wafer for fan-out WLP. Finite Element Method (FEM) was used to reduce wafer warpage by optimizing geometry design, matching the CTE of carrier and EMC, balanced RDL design and low shrinkage dielectric, low ratio of die to package area and use of low molding temperature.

Die shift during molding is one of the biggest issues in WLCSP. Dies shift will cause misalignment in subsequent RDL lithography process. Khong *et al.,* [12] analyzed die shift for die with size 5mm x 5mm using computational fluid dynamic (CFD) simulation coupled with structural analysis. The study found that the die shift increased when the thinner dies was used, higher mold compound fluid velocity and increase of pitch of dies. Mazuir *et al.,* [13] studied optimization method for die shift by adjusting the adhesion level of silicon dies on the carrier support. Die shear was used to characterize the adhesion of silicon die on adhesive and pick and place condition where the force applied on the dies was optimized to improve the die shift significantly.

Above literature survey shows reseachers had enthusiastically overcome reliability and processes challenges in CSP for semicondoctor packaging. FEM and CFD had been deployed to understand the process settings on CSP during assembly and improvw the processes during the development stage. However, very few papers in literature discussed about CSP architecture in Light Emitting Diode.

1.2 CSP in Light Emitting Diodes (LED)

Light emitting diode (LED) which is an eco-friendly technology has been in the mainstream of lighting products replacing conventional lighting technology of incandescent bulbs and fluorescent lamps. LED is more energy efficient, lower cost and long lasting.

Package miniaturization, improvement of thermal management, higher reliability, and the criticality of connecting ever increasing pin-count on an ever shrinking die are the main drivers for CSP development in Integrated ICs. The development started in late 1990s and achieved high volume manufacturing maturity around 2000s. A CSP is an individual chip which can be directly mounted to printed circuit board (PCB) and has the same size as the chip. For LED devices, CSPs normally are made of flipchip LED die on which a phosphor layer is coated. CSP packaging has simplified assembly

process steps compared to conventional LED packaging using ceramic substrate and molded encapsulant as optic lens. This has also enabled simplified LED package integration into LED module.

Lumileds is one of the first company enable commercial CSPs to the market. In year 2014, Bhardwaj Jyoti from Lumileds presented detail information about the development of chip scale package technology [14]. Figure 1 below shows evolution of the LED package from traditional leadframe to CSPs. He added that current technology trend with high power LEDs are using thin film die mounted on a ceramic package. Lateral die with two wirebonds for contacts in lead frame or QFN packages with dispense phosphor are the major technology which dominating mid and low power LED. Bhardwaj Jyoti also emphasized this new LED architecture which is flexible enough for both high and mid-power applications is the Flip Chip version of chip scale package (CSP). CSPs have smallest packaging size for applications where optical features such as lens is limited especially for mobile hand phone flash light application.

In 2016, Samsung Electronics Co., Ltd., a world leader in advanced component solutions, announced a new line-up of chip scale package (CSP) LED modules. These CSP LED modules are designed for spotlights and downlights which have advance features such as color tunability [15]. In September 2017, Osram Opto Semiconductors GmbH also followed the trend and announced the Ceramos C chip-scale package (CSP) LEDs made for applications related to flash lights [16].

In Nov 2018, by Transparency Market Research (TMR) titled "Chip Scale Package (CSP) LED Market – Global Industry Analysis, Size, Share, Growth, Trends, and Forecast, 2018–2026." published that the global CSP LED market was valued at US$ 844.2 million in 2016 and is projected to register compound annual growth rate (CAGR) of over 13.90% from 2018 to 2026. The report suggested that chip scale package (CSP) LED had penetrated into automotive, consumer electronics, and media & entertainment industries worldwide market. The rising trend of using technology such as augmented reality or virtual reality around the globe helps to accelerate the demand for chip scale package (CSP) LED in the coming years [17].

Fig. 1. Evolution of leadframe package to CSP in products offering in Lumileds

In 2019, Lumileds once again extended its capability to demonstrate CSP leadership with directional CSPs for smallest and brightest spotlights. Lumileds launched the LUXEON CSP HL1, compact, directional CSPs that provide high lumen density in directed, narrow beams or in ultrahigh density arrays for indoor area lighting. The product line is designed to set new records for shrinking

the footprint of spotlights, wall grazing, wall washing and linear fixtures for architectural, high impact retail, home and office lighting venues. The package size is 1.4mm x 1.4mm x 0.3mm consists of two pads that attach directly to the PCB for ease of SMD assembly and significant reduction of cost [18].

All the big players in LED market already geared up to adopt CSP technology to capture market share in various applications. Time to market, lower cost and reliable CSP products become crucial to gain this exuberant market share in automotive, consumer electronics, and media & entertainment industries worldwide market.

1.3 Molding Process for CSP

Although wafer level packaging technology is well established in semiconductor industry but there are limited papers discuss about its application in LED. Process of wafer reconfiguration is the most practical application for LED [33-36]. The tested good chips are placed metal-up onto a carrier with adhesive tape. The distance between chips or the fan-out area around the chips will determine the package size. Adhesive is used to protect the active area from molding compound.

Compression molding or transfer molding is used to fill the gap between the chips and hold chips and embedded components together. The reconstituted wafer then released from the carrier and proceeds to singulation process. The carrier can be reused and this will drive the cost down dramatically.

There are issues in molding process for WLCSP in semiconductor such as warpage, chips shift, void, stress concentration on chips and solder bumps [38-40]. Finite Element Method had been used to model the shrinkage caused by thermal mismatch of carrier and epoxy mold compound (EMC) which has resulted in chips shift and warpage [38-39]. Chip shift in embedded wafer-level process also occurs during molding process. This is mainly contributed by coupling of coefficient of thermal expansion of different materials and mold flow effect [43]. Fluid–structure interaction (FSI) analysis and Computational Flow Dynamic (CFD) is used to simulate the EMC flow and the effects of solder bump arrangement on pressure distribution, void, deformation, and stress imposed on the IC structures are investigated [40-42].

Bu *et al.,* [19] investigated the non-linear trend of in shift in wafer-level packaging which coupled the effects of coefficient of thermal expansion with mold flow effect. In an experimental inspection, die shift is found to be 75% contributed by CTE effects and 25% by mold flow. CFD analysis with Fluent software was used to simulate the mold flow using mold compound modeled as a shear-rate-dependent viscosity obeying the Cross Model. The output of mold results which is pressure distribution on the walls of the dies is mapped to the dies in ABAQUS. Then the CTE and chemical shrinkage is incorporated and simulated using finite element method. The outputs of die shift by FEM agreed well with experiment data. The paper concluded that filling speed, molding time, initial thickness and initial diameter of the mold compound are the parameters to be optimized to minimize the die shift.

Ji *et al.,* [20] developed a 3-D numerical method to simulate the flow of compression molding for multichip embedded WLP. The paper reported two main issues in compression molding which are incomplete fill and die sliding. The paper used ANSYS Fluent 13.0 to simulate flow pattern during molding. Mold compound was treated as a shear-thinning generalized Newtonian fluid and Castro-Macosko model was used to simulate the viscosity of model. The curing effect of the polymer molding was neglected as the compression stage is less than 5 seconds. The short shot was used to validate the simulation result. The paper concluded that the incomplete fill can be eliminated by symmetrical design which led to symmetrical resistance for mold flow in x and y direction. The paper proposed to

use the slower compression speed at the end of the process and increase the contact area between die surfaces with mold tape to reduce die slide.

Han *et al.,* [21] highlighted that compression molding process in fan-out wafer level packaging (FOWLP) had induced die shift. He had developed multi-step simulation to evaluate the die shift variation at different processes. They developed 3D simulation models to quantify thermal–mechanical effect and fluid flow effects using COMSOL Multi-physic FEM software. 5 loading steps included heating up from room temperature at 25°C to molding temperature of 125°C, solidified mold compound cooled down to warm temperature of 40°C, heating up to the thermal release temperature, thermal temperature of post mold curing temperature and cooling from post mold curing temperature to room temperature. The last 2 steps normally induced die shift because of thermal mismatch of the whole system and chemical shrinkage of mold compound. To reduce the fluid flow effect, thick mold compound, thinner die and higher temperature were suggested. This paper suggested low tape releasing temperature, higher glass transition tape, smaller CTE mold compound and Si mold plate could reduce the thermal-mechanical effect and help in smaller die shift. Other improvement suggested are using higher adhesive, bigger die and die shift compensation using dynamic pre-shift the die which can help to reduce maximum die shift under +/-10um.

Yeon *et al.,* [22] studied the die shift for WLP using compression molding. Die shift was found as the major defects which prevented high yield production. The die shift caused by the drag force of the epoxy mold compound was measured and determined analytically. Thermal contraction/expansion and warpage are the culprit of die movements. The regression model was built to predict the die shift due to flow drag force and the data was used to do die realignment to compensate the die shift.

Most of the papers discussed mold flow and mechanical simulation using encapsulation made of EMC as it is common in semiconductor industry. In LED packaging, silicone is used in encapsulation process due to its better thermal and light resistance [44]. Silicone used in LED especially for CSP with sapphire are highly filled with fillers such as silica, alumina, and reflective substances. The fillers help to reduce the CTE mismatch of silicone with sapphire. Lower CTE is important to reduce the stress of silicone interface with sapphire which will prevent delamination. Reflective substances added in the silicone help to reflect light to the top surface to increase luminance which is flux per surface area. The added fillers have reduced the compisition of of silicone base resin. This has increased cure rate and higher viscosity during mold flow. When the viscosity of silicone increases it causes higher drag force especially during the end of filling phase.

1.4 Characterization of Encapsulating Material for LED and Electronic Packaging

Light extraction efficiency of LEDs is crucial to improve the performance of packages. The light could be confined within the chip which has refractive index of 2.6 and its huge difference with air. Encapsulating material play important role as a LED housing to extract light. Encapsulating material normally has refractive index of 1.4 – 1.5 which reduce the contrast of refractive difference between chip and air, thus help in extracting the light. Encapsulating materials are generally categorized into two groups which are epoxy-based and silicone-based. Typical epoxy chemical structure is as Figure 2.

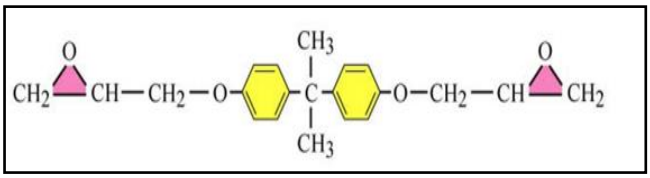


Fig. 2. Typical epoxy chemical structure for semiconductor packaging

Epoxy normally has good mechanical stability and lower cost. However, epoxy will become yellowing under the long exposure of heat and UV light under testing. Degradation happened because during rearrangement of structures along the backbone of polymer forming peroxide and build-up of radicals [23]. In long term exposure of UV light silicone-based encapsulating materials have excellent thermal stability against yellowing [44]. Silicones are materials consisting of pendant organic groups along the inorganic siloxane backbone (Si-O-Si-). Silicone could be represented by structure in Figure 3.

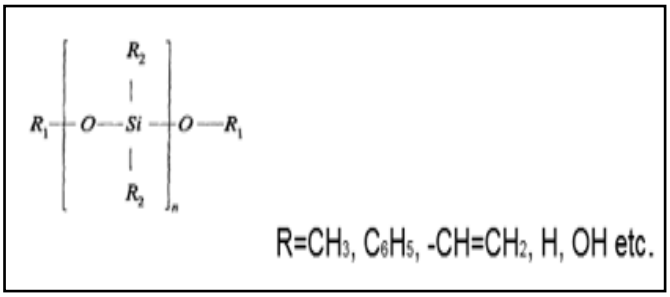


Fig. 3. Silicone chemical structure for LED applications

Various functional moieties like epoxy, amine, hydroxyl, vinyl, acryl can be introduced along the main chain or as side groups to form novel polymers [26]. Fillers such as silica are added into the silicone system to improve the mechanical properties such as reducing CTE, improve toughness, elongation, tear and thermal conductivity [27]. Other optical functional substances such as TiO_2 nanoparticles are doped into the silicone to encapsulate GaN-based LEDs to increase the refractive index and improve the light extraction efficiency of LEDs [27,28].

However, increase of fillers will increase the viscosity of the silicone. Hamidi *et al.,* [30] found that the addiction of fillers such as nanoclay increases the bulk viscosity of the polymer and causing excessive pressure required for injection molding and void occurrence found to be increased with the increase of fillers. Higher viscosity will cause higher pressure and viscous in molding process. Ong *et al.,* [45] studied the implication of rheological behavior of EMC towards 3D IC packaging. The EMC rheological characteristic posed significant impact and fluid flow behavior during plastic encapsulation process. The viscous flow found to be unfavorable due to low filling rate, more air entrapment and higher pressure distribution, which prone to deflect the delicate 3D die with Through Silicon Via (TSV) and eventually causes reliability issue.

Hence rheological characterization of material especially the reactive viscosity and curing kinetic is important for moldflow simulation and selection of silicone in LED packaging. Khor *et al.,* [31] had done comprehensive literature review on fluid-structure interaction modelling challenges in IC packaging during encapsulation process. In the review, governing equations and viscosity model used in the moldflow simulation were briefly discussed. Castro-Macosko model found to be adequate to describe the influence of polymerization towards viscosity of molding material. Kamal equation is incorporate into the Castro-Macosko model to describe the curing kinetics of mold material and its

influences in flow viscosity. Viscosity of the flow corresponding to curing behavior and mold temperature which happened during process due to chemical reaction of mold material which could be obtained by rheological characterization. Rheological measurement could be carried out using rheometer and differential scanning calorimeter.

Lai *et al.,* [32] studied the rheokinetic characterization of epoxy molding compound (EMC) using Kamal's model and Cross Castro-Mascoko model. The fitted parameters in both models then used for transfer molding simulation by Moldex3D for Dual side System in Package application. The molding simulation result was compared with actual voids locations and short shots and had good agreement. The simulation helped to optimize design and process parameters in enhancing flow balance, reduce voids and device defects.

Dreissigacker *et al.,* [33] studied compression molding with liquid encapsulants which focus is set on forces exerted on individual dice during encapsulation in fan-out wafer-level packaging (FOWLP). Analytical approach had been developed to calculate the melt front velocity and simulations carried out to capture the nonlinear kinematics, chemorheology using Castro-Mascoko model, and to extract forces exerted on individual dice. Optimization of process parameters, such as compression speed, and process temperature, are determined to minimize the forces on the dice which causes drag forces exceed adhesive forces. This approach had helped to minimize flying dies and improve yield performance.

Ishak *et al.,* [49] evaluated influence of stacking chips arrangement during encapsulation process. The encapsulation process was simulated using computational fluid dynamic software (Fluent) while structural analysis are using finite element method software (STRUCTURAL). The Castro-Macosko and Kamal models are used to describe the non-Newtonian behavior and the curing kinetics of the epoxy molding compound (EMC) in the Fluent software.

Lin *et al.,* [34] developed simulation molded underfill (MUF) using compression molding for SiP assembly process using Moldex3D software. In paper, authors apply Kamal's model to govern curing effects and Castro-Mascoko model to govern rheology characteristic of the EMC. The study helped to determine the factors in bump and die geometry that contributed to void formation during filling process. Design rule had been established to minimize the void formation in the MUF.

Ng *et al.,* [50] investigated the flow simulation using ANSYS Fluent for underfill flow. Due to high computational time for flip-chip underfill encapsulation process, the researchers presented a new symmetrical unit-cell approach. The approach help to reduce the computational while with minimum discrepancy with experimental data by not more than 14.54%.

1.5 Conclusion from Literature Survey

CSP in LED is an exciting trend and compression molding is feasible and low cost molding process for CSP. There are limited papers in literature discussing about FSI analysis on silicone resin and its implication to CSP for LED. As such, the aim of this paper is to discuss about the application of virtual prototyping or computer aided engineering (CAE) in CSP during the design stage, from the aspects of thermal stress and mold flow effect.

EMC is widely used in electronic packaging, hence Kamal's model and Castro-Mascoko model are generally utilized to describe the curing kinetic and rheology behaviour of EMC respectively. The moldflow of silicone in CSP for LED is almost non existence in open literature The method to characterize silicone material to obtain curing kinetics of silicone and reactive viscosity which dependent on degree of curing is not included in most of the study.

As such, CFD and FSI are employed in the development prior to real material testing which is time consuming, labor intensive and costly especially if new mold cavities are required. CFD allows us to

understand the flow pattern of the silicone and the interaction between the silicone viscosity and the molding parameters. Viscosity of the fluid is a complex function of the temperature, shear rate and degree of chemical reaction. Hence, a complete parametric study of mold parameters for the silicone of interest can help prevent air trap, incomplete mold (shorts shot), weld line and unbalance flow. On the other hand, FSI basing on the input from CFD provides insight into the effect of mold flow onto chips offsets, mold crack and wafer warpage. In this project, Autodesk Moldflow is employed. It combines both the function of CFD and FSI.

2. Methodology and Results

2.1 Thermal Stress

Chip displacement is the major issue in CSP using reconfiguration wafer level CSP. Chip displacement is due to two reasons which are the flow of silicone and the CTE difference between the material in assembly. Among all materials in assembly, silicone has the highest CTE value. The high CTE and curing shrinkage of silicone cause the material to shrink and pulls the chips into the center of the wafer during the cool down from molding temperature to the room temperature. FEM is used to analyze the chip displacement with different silicone and assist engineer to choose the reliable material which reduces chip displacement. Table 1 shows normalized Young's modulus and normalized CTE of silicone A and silicone B. The value of the Young's modulus is normalized based on Silicone A at 25^{o}C. The value of the Coefficient of Thermal Expansion is normalized based on Silicone A at 25^{o}C

Table 1
Material properties for different silicone materials

Material	Temprature (°C)	Normalized Young's Modulus	Normalized Coefficient of Thermal Expansion
Silicone A	25	1	1
	100	0.071	2.5
	200	0.071	2.5
Silicone B	25	39.41	0.375
	100	4.12	1.25
	200	4.12	1.25

Figure 4 shows the result of silicone shrinkage with the change of curing temperature 150^{o}C cooling down to 25^{o}C. Deformation of silicone is prominent and it moves the chips inward to the center of the substrate. Taking an example of specification from customer for LED placement accuracy has to be within certain tolerance, the regions of orange and red color in Figure 4 are not acceptable. The black color square is representing the LED chips area. Silicone A showing high yield loss during assembly due to the shrinkage of silicone and silicone B showing better yield as the orange and red area is out of the boundary of LED chips area.

FEA enables design engineer and mold engineer to discover the root cause of LED chips displacement. The thermal stress analysis help development engineers select the optimum material to improve the process yield in mass production without experimenting different material.

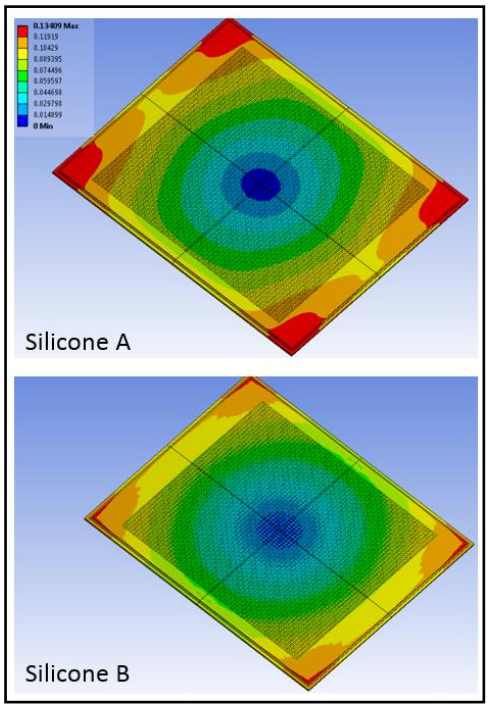


Fig. 4. Deformation contour of silicone

2.2 Silicone Material Characterization

Material characterization to obtain the reaction kinetic and rheological properties is crucial as inputs to the simulation for accurate prediction of mold flow. Measurement instruments such as Differential Scanning Calorimetry (DSC) and Rheometer are used to characterize the reactive curing and dynamic viscosity of the silicone.

Silicone is a thermoset material and can be processed in partial polymerized silicone molding compound. Polymerization starts when the silicone in the cavity melts and with the applied molding pressure, it fills up the cavity. Chemical cross-linking happens during the flow causing a change in viscosity, shear rate and hence the flow behavior of the silicone. The chemical reactions that occur during filling and curing further add complexity to molding process.

Various empirical models have been developed to derive the degree of cure kinetics. Horie *et al.,* had developed an isothermal approach basing on autocatalytic model and this model was extended by Kamal. The model accounts for an autocatalytic and non-autocatalytic reaction in which the initial reaction rate is not zero.

$$\frac{d\alpha}{dt} = (K_1 + K_2\alpha^m)(1-\alpha)^n \tag{1}$$

α is the degree of cure corresponding to the $d\alpha/dt$ rate and denotes the conversion time of silicone groups at a given time, t. K_1 is the rate constant of the reaction of partial order *n* catalyzed by an accelerator. K_2 is the rate constant of the autocatalytic reaction of partial order *m*. The Kamal K_1 and K_2 are specific rate constants which follow an Arrhenius shape and are temperature dependent, as describes by the equation below

$$K_1 = A_1 \exp\left(\frac{-E_1}{RT}\right) \text{ and } K_2 = A_2 \exp\left(\frac{-E_2}{RT}\right) \tag{2}$$

For rheological properties, reactive viscosity is utilized to describe the temperature, shear rate and cure dependence of thermoset material. It is described by the equation below

$$\eta\left(\alpha,T,\dot{\gamma}\right)=\frac{\eta_0(T)}{1+\left(\frac{\eta_0(T)\dot{\gamma}}{\tau^*}\right)^{(1-n)}}\left(\frac{\alpha_g}{\alpha_g-\alpha}\right)^{(C_1+C_2\alpha)} \tag{3}$$

η is the viscosity, $\dot{\gamma}$ is the shear rate, T is the temperature, α is the degree of cure and $\eta_0(T)=B\exp\left(T_b/T\right)$ and n, τ^*, B, T_b, b, C_1, C_2, α_g and g (gelation conversion) are data-fitted coefficients.

2.3 Simulation Setup and Result

Autodesk Moldflow is utilized to predict the fluid flow for compression mold. Material from Autodesk Moldflow library is used. The responses are the fill time, crack line, void formation and chips displacement when the silicone complete fill the mold cavity.

Some of the key assumptions were made to simplify the model and reduce computational time. As shown in Figure 5, the model consists of specified locations of chips with tablet of silicone mold compound (in blue) placed at the center of the frame. Only two rows and columns of chips at the frame peripheral and a row of chips at the middle of frame was modeled. This is because the peripheral areas are vulnerable to chips displacement as the degree of curing is the highest at region farthest away from the tablet location. When the mold compound starts to cure, the increase in viscosity will result in high shear force and displace the chips. Hence, the middle row of the chips is modeled so as to evaluate the effects of viscosity of the mold compound on chips displacement during melting process. Chips at other locations are represented by four dummy big blocks (in blue).

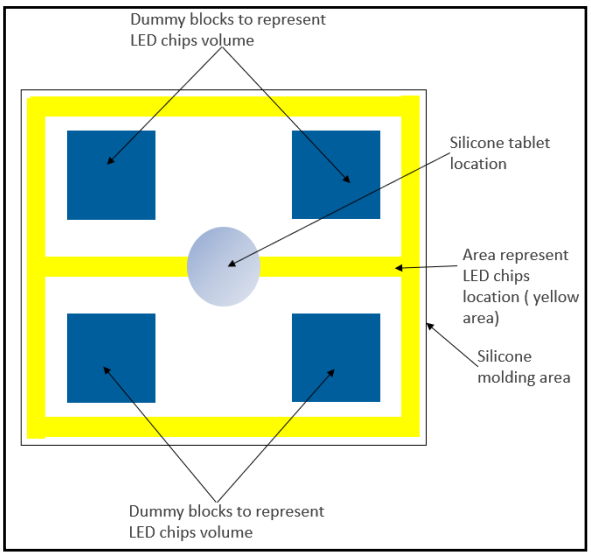


Fig. 5. Model setup for mold simulation

Temperature of the cavity and molding speed were altered in this study. Table 2 shows the Design of Experiment (DoE) for temperature and injection time. Injection time is the time needed for the movement of the bottom mold chase to reach the final stage as shown in Figure 6. The response of the DOE is chips displacement.

Table 2
DoE to improve chips displacement

Experiment	Temperature (°C)	Injection time (s)
1	To	t
2	To-15	t
3	To-15	t-6
4	To-15	t-12

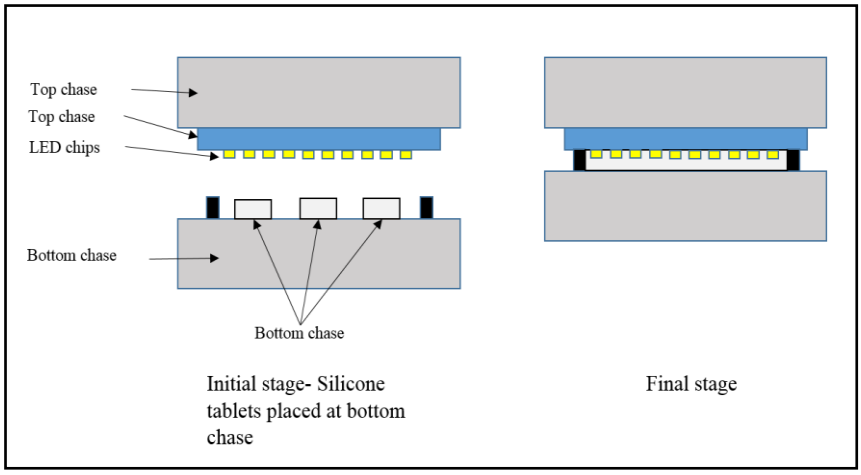


Fig. 6. Illustration of bottom chase travel from initial stage to final stage

Figure 7 below shows the pattern of flow front during the compression molding. Short shot was used to confirm if the flow pattern of simulation is the same as the actual. Observation of filling will help engineers to adjust the molding speed and hence to improve the flow if there are failures like void and crack.

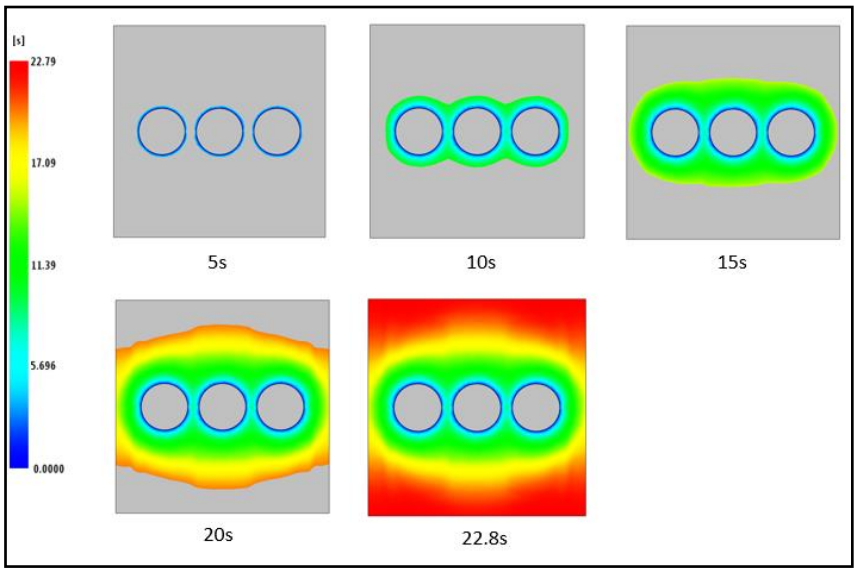


Fig. 7. The flow of silicone with respect to filling time for experiment 1

Figure 8 shows the displacement of LED chips for four different condition in Table 2. In Table 2, *To* represent original temperature and *t* represent original injection time. The red box in figure 8 shows the area of interest for LED chips displacement as the silicone starts to cure and increase in viscosity when it travels to the corner of the frame. Figure 9 shows that decreasing the temperature and reduce the injection time minimize the displacement of the LED chips. Experiment 1 had exhibited highest chips displacement at 230um and improved to 138um in experiment 4.

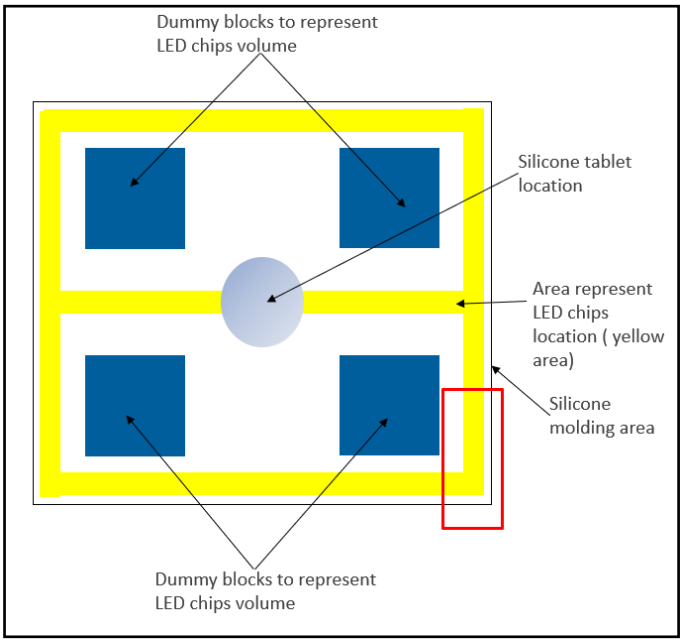


Fig. 8. Area of Interest for chips placement in red box

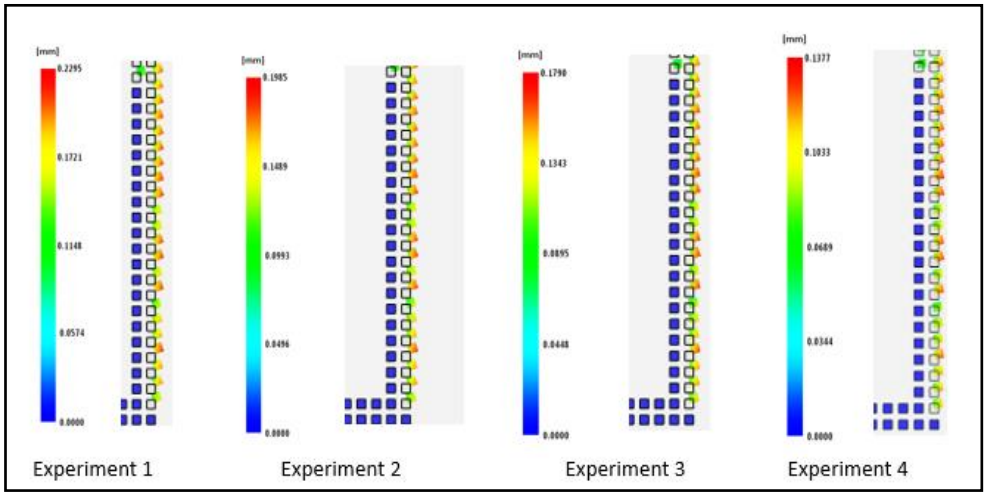


Fig. 9. Contour Plots of Chips Placement

Reducing the mold temperature reduces curing rate of the silicone hence maintaining it at the lowest viscosity. LED chips placement is able to improve by pushing silicone with lowest viscosity as fast as possible to the corner of the frame with decrease of injection time. Autodesk Moldflow also able to provide plot of flow velocity, temperature, air traps and weld line formation at certain time such as in Figure 10 which could help engineers to optimize the process settings and material selection. Red circle in Figure 10 (c) shows the potential air trap area but it is outside the chips area. Air traps happens due to improper vent design and will cause void and becomes crack initiation point.

Red rectangle in Figure 10 (d) shows the weld line formed due to melt flow fronts collide in mold cavity and it can significantly weaken the structural integrity of the molded parts. CFD is able to detect the potential failures and reduces the numbers of experiment and narrow down the scope of material selection in molding process which require high cost.

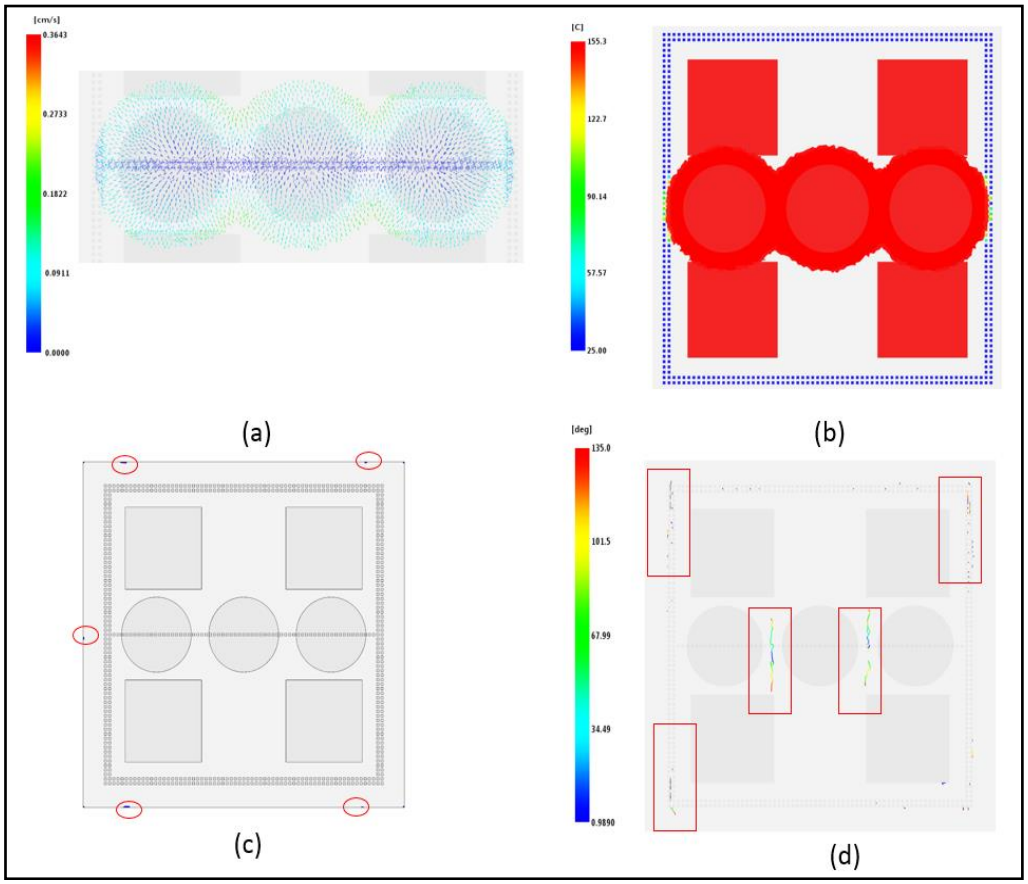


Fig. 10. (a) Front flow velocity at 10s (b)Temperature distribution of fluid and chips at 10s (c) Air traps formation (d) Weldline formation

3. Conclusion

This paper had shown various way how virtual prototyping via CFD and FEM to help to optimize the process settings and material selection. Virtual prototyping has provided understanding of multiphysic phenomenal in CSP LED in term of thermal stress and molding process in LED CSP development. Virtual prototyping reduces the labor intensive and huge investment in complex experiment, toolings and material to enable high yield, low cost and good reliability product in LED CSP, hence accelerates the product development to market cycletime.

References

[1] Garrou, Philip. "Wafer level chip scale packaging (WL-CSP): an overview." *IEEE Transactions on Advanced Packaging* 23, no. 2 (2000): 198-205. https://doi.org/10.1109/6040.846634
[2] Shu, Huihua. "Enhanced Polymer Passivation Layer for Wafer Level Chip Scale Package." PhD diss., 2011.
[3] SRINIVASARAO, VEMPATI. "Bed of nails (B0N)-100 microns pitch wafer level off-chip interconnects for microelectronic packaging applications." (2005).
[4] Huffman, Alan, and Philip Garrou. "Status, and Future of Flip Chip & Wafer Level Packaging." *International Symposium on Microelectronics* 2010, no. 1 (2010): 325-332. https://doi.org/10.4071/isom-2010-TP5-Paper1
[5] Burggraaf, Pieter. "Chip scale and flip chip: attractive solutions." *Solid state technology* 41, no. 7 (1998): 239-244.

[6] Ebin, Liao. "Compliant Chip-to-Package Interconnects for Wafer Level Packaging." (2008).
[7] Fan, X. J., B. Varia, and Q. Han. "Design and optimization of thermo-mechanical reliability in wafer level packaging." *Microelectronics Reliability* 50, no. 4 (2010): 536-546. https://doi.org/10.1016/j.microrel.2009.11.010
[8] Rogers, Boyd, Chris Scanlan, and Tim Olson. "Implementation of a fully molded fan-out packaging technology." In *IWLPC*, (2013). https://doi.org/10.1109/TCPMT.2019.2935477
[9] Che, F. X. "Study on board level solder joint reliability for extreme large fan-out WLP under temperature cycling." In *2016 IEEE 18th Electronics Packaging Technology Conference (EPTC)*, (2016): 207-215. https://doi.org/10.1109/EPTC.2016.7861473
[10] Kripesh, Vaidyanathan, Vempati Srinivas Rao, Aditya Kumar, Gaurav Sharma, Khong Chee Houe, Zhang Xiaowu, Khoo Yee Mong, Navas Khan, and John Lau. "Design and development of a multi-die embedded micro wafer level package." In *2008 58th Electronic Components and Technology Conference* IEEE, (2008): 1544-1549. https://doi.org/10.1109/ECTC.2008.4550181
[11] Che, F. X., David Ho, Mian Zhi Ding, and Xiaowu Zhang. "Modeling and design solutions to overcome warpage challenge for fan-out wafer level packaging (FO-WLP) technology." In *2015 IEEE 17th Electronics Packaging and Technology Conference (EPTC)*, (2015): 1-8. https://doi.org/10.1109/EPTC.2015.7412319
[12] Khong, Chee Houe, Aditya Kumar, Xiaowu Zhang, Gaurav Sharma, Srinivasa Rao Vempati, Kripesh Vaidyanathan, John Hon-Shing Lau, and Dim-Lee Kwong. "A novel method to predict die shift during compression molding in embedded wafer level package." In *2009 59th Electronic Components and Technology Conference*,Proc. *IEEE/ECTC* (2009): 535-541. https://doi.org/10.1109/ECTC.2009.5074066
[13] Mazuir, J., V. Olmeta, M. Yin, G. Pares, A. Planchais, K. Inal, and M. Saadaoui. "Evaluation and optimization of die-shift in embedded wafer-level packaging by enhancing the adhesion strength of silicon chips to carrier wafer." In *2011 IEEE 13th Electronics Packaging Technology Conference*, pp. 747-751. IEEE, (2011): 747-751. https://doi.org/10.1109/EPTC.2011.6184519
[14] www.ledinside.com/knowledge/2013/12/philips_lumileds_chip_scale_packaging_for_leds
[15] news.samsung.com/us/samsung-introduces-full-line-led-components-based-chip-scale-packaging-technology/
[16] www.ledinside.com/products/2017/9/mini_led_for_mobile_devices_osram_launches_compact_ceramos_generation
[17] www.transparencymarketresearch.com/pressrelease/chip-scale-package-led-market.htm
[18] www.lumileds.com/news/347/50/Lumileds-Demonstrates-Chip-Scale-Package-CSP-Leadership-with-Directional-CSPs-for-Smallest-Brightest-Spotlights
[19] Bu, Lin, Siowling Ho, Sorono Dexter Velez, Taichong Chai, and Xiaowu Zhang. "Investigation on die shift issues in the 12-in wafer-level compression molding process." *IEEE Transactions on components, packaging and manufacturing technology* 3, no. 10 (2013): 1647-1653. https://doi.org/10.1109/TCPMT.2013.2268192
[20] Ji, Lin, Dexter Velez Sorono, Tai Chong Chai, and Xiaowu Zhang. "3-D numerical and experimental investigations on compression molding in multichip embedded wafer level packaging." *IEEE Transactions on components, packaging and manufacturing technology* 3, no. 4 (2012): 678-687. https://doi.org/10.1109/TCPMT.2012.2220141
[21] Han, Yong, Mian Zhi Ding, Bu Lin, and Chong Ser Choong. "Comprehensive investigation of die shift in compression molding process for 12 inch fan-out wafer level packaging." In *2016 IEEE 66th Electronic Components and Technology Conference (ECTC)*, (2016): 1605-1610. https://doi.org/10.1109/ECTC.2016.46
[22] Yeon, Simo, Jeanho Park, and Hye-Jin Lee. "Compensation method for die shift caused by flow drag force in wafer-level molding process." *Micromachines* 7, no. 6 (2016): 95. https://doi.org/ 10.3390/mi7060095
[23] Krauklis, Andrey E., and Andreas T. Echtermeyer. "Mechanism of yellowing: Carbonyl formation during hygrothermal aging in a common amine epoxy." *Polymers* 10, no. 9 (2018): 1017. https://doi.org/10.3390/polym10091017
[24] Luo, Xiao, Jiajie Fan, Mengni Zhang, Cheng Qian, Xuejun Fan, and Guoqi Zhang. "Degradation mechanism analysis for phosphor/silicone composites aged under high temperature and high humidity condition." In *2017 18th International Conference on Electronic Packaging Technology (ICEPT)*, (2017): 1331–1336. https://doi.org/10.1109/ICEPT.2017.8046684
[25] Yazdan Mehr, Maryam, Willem Van Driel, Francois De Buyl, and Kouchi Zhang. "Study on the degradation of optical silicone exposed to harsh environments." *Materials* 11, no. 8 (2018): 1305. https://doi.org/10.3390/ma11081305
[26] JOHANNES, KARL. *Reactive Polymers: Fundamentals and Applications*. William Andrew Publishing, 2017.
[27] Kong, S. M., M. Mariatti, and J. J. C. Busfield. "Effects of types of fillers and filler loading on the properties of silicone rubber composites." *Journal of reinforced plastics and composites* 30, no. 13 (2011): 1087-1096. https://doi.org/10.1177/0731684411416267
[28] Wang, Pin-Chao, Chun-Liang Lin, and Yan-Kuin Su. "Enhancement of light extraction efficiency in GaN-based blue light-emitting diodes by doping TiO2 nanoparticles in specific region of encapsulation silicone." *Japanese Journal of Applied Physics* 52, no. 8S (2013): 08JG15. https://doi.org/10.7567/JJAP.52.08JG15

[29] Momen, Gelareh, and Masoud Farzaneh. "Survey of micro/nano filler use to improve silicone rubber for outdoor insulators." *Rev. Adv. Mater. Sci* 27, no. 1 (2011): 1-13.
[30] Hamidi, Youssef K., Levent Aktas, and M. Cengiz Altan. "Effect of nanoclay content on void morphology in resin transfer molded composites." *Journal of Thermoplastic Composite Materials* 21, no. 2 (2008): 141-163. https://doi.org/10.1177/0892705707083635
[31] Khor, C. Y., Mohd Zulkifly Abdullah, Chun-Sean Lau, and I. A. Azid. "Recent fluid–structure interaction modeling challenges in IC encapsulation–A review." *Microelectronics Reliability* 54, no. 8 (2014): 1511-1526. https://doi.org/10.1016/j.microrel.2014.03.012
[32] Lai, Jin-Yuan, Tang-Yuan Chen, Ming-Han Wang, Meng-Kai Shih, David Tarng, and Chih-Pin Hung. "Characterization of Dual Side Molding SiP Module." In *2017 IEEE 67th Electronic Components and Technology Conference (ECTC)*, (2017): 1039- 1044.
[33] Dreissigacker, Marc, Ole Hoelck, Joerg Bauer, Tanja Braun, Karl-Friedrich Becker, Martin Schneider-Ramelow, and Klaus-Dieter Lang. "A numerical study on mitigation of flying dies in compression molding of microelectronic packages." *Journal of Microelectronics and Electronic Packaging* 16, no. 1 (2019): 39-44. https://doi.org/10.4071/imaps.763387
[34] Lin, YiXuan, Ian Hu, Dao-Long Chen, David Tarng, and C. P. Hung. "Compression Molding Mechanism and Parameter Evaluation of SiP." In *2020 15th International Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT)*, (2020): 116-120. https://doi.org/10.1109/IMPACT50485.2020.9268556
[35] Kim, Hyun Woo, Jongchan Kim, Joonhyuck Lee, Sangsung Park, and Dongsik Jang. "Trend research on flip-chip CSP LED for establishing management of technology strategy." In *Proceedings of International Conference on Economics and Business Management*, (2015): 146-151.
[36] Fan, Xuejun. "Wafer level packaging (WLP): fan-in, fan-out and three-dimensional integration." In *2010 11th International Thermal, Mechanical & Multi-Physics Simulation, and Experiments in Microelectronics and Microsystems (EuroSimE)*, (2010): 1-7. https://doi.org/10.1109/ESIME.2010.5464548
[37] Brunnbauer, Markus, Thorsten Meyer, G. Ofner, K. Mueller, and R. Hagen. "Embedded wafer level ball grid array (eWLB)." In *2008 33rd IEEE/CPMT International Electronics Manufacturing Technology Conference (IEMT),* (2008): 1-6. https://doi.org/10.1109/EPTC.2008.4763559
[38] Keser, Beth, Craig Amrine, Trung Duong, Owen Fay, Scott Hayes, George Leal, William Lytle, Doug Mitchell, and Robert Wenzel. "The redistributed chip package: A breakthrough for advanced packaging." In *2007 Proceedings 57th Electronic Components and Technology Conference*, (2008): 286-291. https://doi.org/10.1109/ECTC.2007.373811
[39] Fan, Xuejun. "Wafer level system packaging and integration for solid state lighting (SSL)." In *2012 13th International Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems*, (2012): 1-6. https://doi.org/10.1109/ESimE.2012.6191771
[40] Bu, Lin, Siow Ling Ho, Sorono Dexter Velez, and Daniel Rhee Min Woo. "Optimization of the wafer level molding process for high power device module." In *2014 IEEE 16th Electronics Packaging Technology Conference (EPTC)*, (2014): 747-751. https://doi.org/ 10.1109/EPTC.2014.7028368
[41] Khong, Chee Houe, Aditya Kumar, Xiaowu Zhang, Gaurav Sharma, Srinivasa Rao Vempati, Kripesh Vaidyanathan, John Hon-Shing Lau, and Dim-Lee Kwong. "A novel method to predict die shift during compression molding in embedded wafer level package." In *2009 59th Electronic Components and Technology Conference*, (2009): 535-541. https://doi.org/10.1109/ECTC.2009.5074066
[42] Chong, Ser Choong, Chee Houe Khong, Keith Lim Cheng Sing, David Ho Soon Wee, Calvin Teo Wei Liang, Vincent Lee Wen Sheng, Kim Hyoung Joon, Jaesik Lee, and Vempati Srinivasa Rao. "Process challenges and development of eWLP." In *2010 12th Electronics Packaging Technology Conference*, (2010): 527-531. https://doi.org/10.1109/EPTC.2010.5702696
[43] Ong, Ernest ES, M. Z. Abdullah, C. Y. Khor, W. K. Loh, C. K. Ooi, and R. Chan. "Fluid–structure interaction analysis on the effect of chip stacking in a 3D integrated circuit package with through-silicon vias during plastic encapsulation." *Microelectronic Engineering* 113 (2014): 40-49. https://doi.org/10.1016/j.mee.2013.07.011
[44] Karlicek, Robert F. "High power LED packaging." In *Conference on Lasers and Electro-Optics*, (2005): 337-339. https://doi.org/10.1109/CLEO.2005.201771
[45] Ong, Ernest ES, Mohd Zulkifly Abdullah, W. K. Loh, C. K. Ooi, and R. Chan. "FSI implications of EMC rheological properties to 3D IC with TSV structures during plastic encapsulation process." *Microelectronics Reliability* 53, no. 4 (2013): 600-611. https://doi.org/10.1016/j.microrel.2012.10.015
[46] Khor, C. Y., Mohd Zulkifly Abdullah, Chun-Sean Lau, W. C. Leong, and MS Abdul Aziz. "Influence of solder bump arrangements on molded IC encapsulation." *Microelectronics reliability* 54, no. 4 (2014): 796-807. https://doi.org/10.1016/j.microrel.2013.12.010

[47] Bu, Lin, Siowling Ho, Sorono Dexter Velez, Taichong Chai, and Xiaowu Zhang. "Investigation on die shift issues in the 12-in wafer-level compression molding process." *IEEE Transactions on components, packaging and manufacturing technology* 3, no. 10 (2013): 1647-1653.. https://doi.org/10.1109/TCPMT.2013.2268192

[48] Zhang, Qin, Xiu Mu, Kai Wang, Zhiyin Gan, Xiaobing Luo, and Sheng Liu. "Dynamic mechanical properties of the transparent silicone resin for high power LED packaging." In *2008 International Conference on Electronic Packaging Technology & High Density Packaging*, (2008): 1-4. https://doi.org/10.1109/ICEPT.2008.4607073

[49] Ishak, Mohammad Hafifi Hafiz, Farzad Ismail, Mohd Zulkifly Abdullah, Mohd Sharizal Abdul Aziz, Hamid Yusoff, Mat Tena'ain, Najib Saedi, and Abdul Hamid. "Fluid–Structure Interaction Study of IC Stacking Chips Arrangement During Encapsulation Process." *CFD Letters* 11, no. 4 (2019): 1-15.

[50] Ng, Fei Chong, Mohd Hafiz Zawawi, Lun Hao Tung, Mohamad Aizat Abas, and Mohd Zulkifly Abdullah. "Symmetrical unit-cell numerical approach for flip-chip underfill flow simulation." *CFD Letters* 12, no. 8 (2020): 55-63. https://doi.org/10.37934/cfdl.12.8.5563