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Experimental Investigation of Heat Transfer from Symmetric and Asymmetric IC Chips Mounted on the SMPS Board with and without PCM

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ABSTRACT

In the present study the experiments were conducted on steady-state that incorporated nine symmetric and asymmetric separate discrete integrated circuits (ICs), strategically positioned at different locations on a substrate board, both with and without phase-change material (PCM). These ICs were subjected to varying levels of heat flux. It has been noted that the temperature is highly influenced by variables such as the size and positions of integrated circuits (ICs), the heat flux applied to the ICs. Furthermore, the non-dimensional geometric distance parameter, λ, is notably affected by both the size and positioning of the ICs. It's observed that at a higher value of λ (0.19), the temperature decreases by 18.79% at a velocity of 3 m/s and by 26.48% at a velocity of 5 m/s without PCM. With PCM, the temperature drop is 23.58% at 3 m/s and 32.47% at 5 m/s. The correlation shows a regression of 0.97 and an RMS error of 0.012%. A proposed correlation establishes a connection between θ (non-dimensional temperature) and λ, suggesting that the maximum non-dimensional temperature (θ) decreases with an increase in λ. This implies that the maximum temperature of the integrated circuits (ICs) is reduced at higher λ values. These findings provide valuable insights for thermal design engineers, aiding them in optimizing the placement of integrated circuits (ICs) to improve the reliability and lifespan of the ICs.

1. Introduction

Electronic industries' rapid expansion and space optimization efforts shrink component sizes, boosting heat generation, challenging reliability. Cooling innovation crucial. Optimizing thermal management crucial for device performance and durability, preventing failure due to elevated operational temperatures. This work focuses on assessing the efficacy of heat sinks in dissipating heat from these chips, crucial for maintaining optimal operating temperatures. By exploring heat sink-

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driven cooling strategies, the aim is to enhance the overall thermal management of integrated circuits. This involves investigating the cooling efficiency and potential temperature reduction achieved through the utilization of heat sinks, contributing to advancements in technology and ensuring the sustained performance and reliability of integrated circuitry in various applications.

Ramadhyani *et al.,* [1] computational research of conjugate heat transfer from tiny isothermal heat sources buried in a large substrate discovered that heat transmission is affected by the substrate's thermal conductivity compared to the fluids. Faghri *et al.,* [2] computed turbulent flow in heated rectangular blocks. High Reynolds number emerging flow employs a modified Lam-Bremhorst turbulence model. Duct entry length reduces heat source leading edge pressure drop. Culham *et al.,* [3] used Microelectronic Thermal Analyzer to anticipate local chip temperatures using a numerically linked fluid-solid model with arbitrarily positioned heat sources. Chen and Liu [4] optimised forced convection arrangement of 9 heat sources. Center-to-center location optimises heat transfer. Chuang *et al.,* [5] numerically simulated heat transfer in five places using PHOENICS. For all configurations, including vertical, top heat sources had the highest temperature. Furukawa and Yang [6] used SIMPLER numerical approach to solve the governing equations and found that increasing thermal conductivity via board thickness cools chips and maximises heat transfer at chip surfaces. Yadav and Kant [7] used the k-E model to study how the size of the array and the temperature of the substrate affect the rate of heat transfer from a heated module. Hotta *et al.,* [8] found that surface radiation cools discrete heat sources under NC. Hotta and Venkateshan [9] discovered that ANN-GA was more significant. Hotta *et al.,* [10] found that painting discrete heat sources black enhances heat transport and decreases temperature by 15%. Natural and mixed convection heat transfer from five heat sources of varying sizes mounted on a PCB in a vertical channel were evaluated by Hotta *et al.,* [11], who decided that the channel's highest-heating sources should be towards the bottom. Optimized passive cooling was achieved by Baudoin *et al.,* [12] of a source array was flush-mounted on a vertical plate by natural convection and found that vertical spacing must be nearly double horizontal spacing. The ideal arrangement depends on heat source density. The staggered configuration that was developed by Baudoin *et al.,* [13] was the result of mathematically optimising the location of a large number of power electronics components that were cooled. Durgam *et al.,* [14] optimised rectangular heat sources on a PCB board using COMSOL MULTIPHYSICS. Kurhade *et al.,* [15-17] studied numerical study of PCM cooling for smart-phone and thermal performance. Patil *et al.,* [18], and Waware *et al.,* [19,20] provide critical reviews on heat transfer and Heat Transfer Enhancement in Tubular Heat Exchangers with Jet Impingement. Khot Rahul *et al.,* [21-25] explain the investigation on Laser Welding Parameters on the Strength of TRIP Steel. Gadekar *et al.,* [26,27], and Kamble *et al.,* [28] explained Experimental Study on Gear EP Lubricant Mixed with $Al_2O_3/SiO_2/ZrO_2$ Composite Additives to Design a Predictive System. Patil *et al.,* [29] used a water-based Al_2O_3 nanofluid was used in this work to grind materials due to its outstanding convective heat transfer and thermal conductivity qualities. Patil and Hotta [30] all delves into cooling square heat sources, particularly comparing different working fluids. Fluorocarbon liquids are favored for their ability to handle higher heat fluxes due to their high boiling points; liquid jet impingement reduces electronic component temperatures by 80 to 85 degrees Celsius. Rosli *et al.,* [31] explained the mass flow rate variation resulted in overall efficiencies of 90.82%, 90.54%, 90.48%, and 90.46% for 10kg/h, 30kg/h, 50kg/h, and 70kg/h, respectively. Additionally, solar irradiance levels of 200 W/m^2, 450 W/m^2, and 800 W/m^2 yielded overall efficiencies of 91.17%, 90.82%, and 90.33%, respectively. However, increased flow rates necessitate stronger pumps, leading to higher system costs. Kurhade *et al.,* [32] explains CFD Approach for Thermal Management to Enhance the Reliability of IC Chips.

The majority of the analyses involved symmetric IC chips with uniform heat flux distribution. The consideration of both symmetric and asymmetric IC chips is rear in literature. The goal is to find the optimal arrangement of IC chips to minimize their temperature and use of PCM for better thermal control experimentally. The objective is to identify the most effective setup (λ) that will result in the lowest maximum temperature for the integrated circuit (IC).

2. Design of Board and IC Chips on SMPS Board with PCM

There are a total of 170,554 distinct arrangements possible for positioning nine symmetric and asymmetric rectangular heat sources on a PCB. Original substrate board dimension is 269 X 189 X 5 as shown in Figure 1 and the material used is copper cladding. Each arrangement is denoted by a λ, ranging from 0.28 to 1.9 in this particular investigation. To generate these various arrangements and their associated λ values, a MATLAB code is utilized. For the current numerical analysis, 30 diverse configurations are selected randomly from the λ values within the 0.28 to 1.9 range. The λ values is calculated using the expression mentioned below [8].

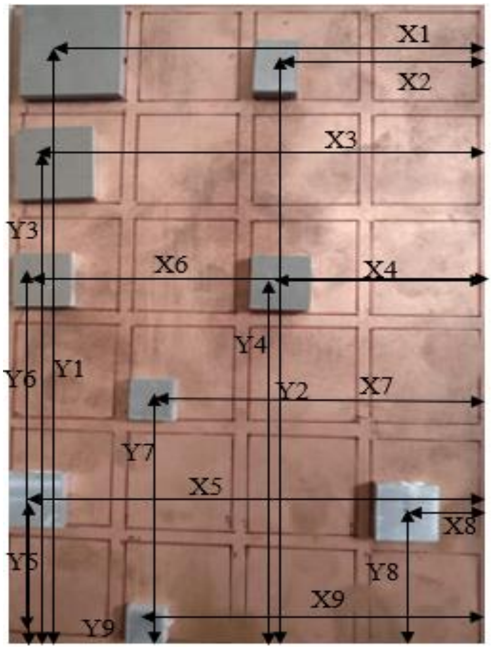

Fig. 1. Positions of IC chips with X and Y coordinates

$$\lambda = \frac{\sum_{i=1}^{9} d_i^2}{l^2 + y_c^2} \tag{1}$$

where,

$$\sum_{i=1}^{9} d_i^2 = (X_i - X_c)^2 + (Y_i - Y_c)^2 \tag{2}$$

$$X_c = \frac{\sum A_i X_i}{\sum A_i} \text{ and } Y_c = \frac{\sum A_i Y_i}{\sum A_i} \tag{3}$$

Table 1 shows the sample calculations of λ values. The 30 configurations are carefully chosen to encompass the entire range of λ values, spanning from 0.28 to 1.9, and they are equally spaced along this range shown in Table 2.

Table 1
Sample calculation of λ values

HS	Xi	L	W	Yi	A	Ai x Xi	Ai x Yi	di^{2}
U1	8.49	35	35	11.2916	1225	10400.3	13832.2	3247.45
U2	9.04	27	27	124.66	729	6590.16	90877.1	5347.65
U3	28.405	15	15	9.43163	225	6391.13	2122.12	2555.56
U4	109.57	12.5	12.5	12.7566	156.25	17120.3	1993.22	6893.51
U5	107.34	19.65	6.5	30.66	127.725	13710	3916.05	5270.09
U6	67.25	15	20	104.39	300	20175	31317	2825.61
U7	105.59	12	20	125.985	240	25341.6	30236.4	8806.3
U8	88.76	20	20	40.52	400	35504	16208	2671.88
Dimensions in mm		Xc = 40.32013		Yc = 58.56104	λ = 1.198			

Table 2
30 different configurations under study

λ	U1-U2-U3-U4-U5-U6-U7-U8-U9	λ	U1-U2-U3-U4-U5-U6-U7-U8-U9
0.280	34-53-33-42-52-34-24-23-61	1.090	11-42-64-31-52-64-14-23-22
0.334	34-21-33-42-52-43-24-23-62	1.144	13-61-52-41-51-14-31-23-14
0.388	14-34-22-42-52-11-24-23-64	1.198	12-61-62-31-52-34-51-23-11
0.442	12-33-41-44-52-33-24-23-63	1.252	11-64-62-32-52-54-12-23-22
0.496	32-43-41-52-53-53-34-23-61	1.306	34-61-12-32-52-14-62-23-13
0.550	33-15-43-52-24-42-11-23-64	1.360	32-64-61-40-52-14-33-23-63
0.604	43-54-42-52-31-21-44-23-64	1.414	22-63-64-42-52-72-63-23-33
0.658	41-52-42-63-51-43-54-23-63	1.468	21-25-64-41-52-62-61-23-33
0.712	43-64-41-52-54-63-34-23-33	1.522	12-63-64-43-52-14-64-23-34
0.766	65-32-43-52-12-44-23-34-61	1.576	33-24-63-41-52-64-61-23-34
0.820	63-42-44-52-32-11-23-14-11	1.630	32-64-63-43-52-62-61-23-34
0.874	34-63-41-52-41-64-23-13-54	1.684	34-61-64-44-52-64-21-23-32
0.928	34-64-43-52-63-42-23-14-11	1.738	11-64-61-44-52-13-62-23-33
0.982	53-64-41-52-62-14-23-54-13	1.792	14-63-12-44-52-61-62-23-32
1.036	14-52-44-52-12-43-63-23-22	1.846	24-61-64-44-52-62-11-23-33

The ceramic brackets are manufactured as per the required dimensions. The positions of IC chips with X and Y coordinates are shown in Figure 1. These brackets are designed and placed on the IC chips on substrate board as shown in Figure 2. The brackets are loaded with PCM in order to improve the operational efficiency of the IC chips. For this study, commercially accessible Paraffin wax has been chosen as the PCM, with a melting point temperature that falls within the range of 48.28°C to 54.21°C. This PCM is initially in a solid state and is subsequently pulverized into a powder form for insertion into the small channels. The thermocouples are inserted at each bracket to measure the channel temperatures and two are immersed inside the PCM to measure their temperature. The completed assembly of the substrate board, containing mini-channels filled with PCM and the thermocouple wires, is employed for the experimental investigation. The electronic components are mimicked with aluminum chip and the thermal conductivity of aluminum is considered.

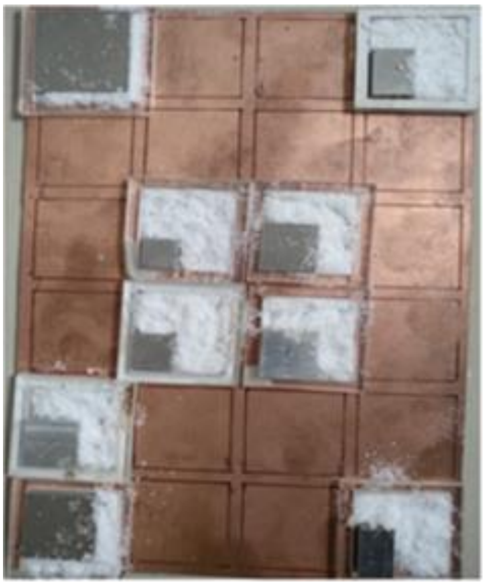

Fig. 2. Board with PCM

Mini channel is surrounded around the periphery of IC chip. The intention behind this proposed design is to absorb maximum amount of heat generated from the heat source by means of direct conduction and reduce temperature across the system. The mini channel is poured with different types of PCM which is classified based on its melting point. The different types of PCM include Paraffin wax, non-paraffin organics, Hydrated salts, and Metals. Paraffin wax is the preferred candidate for our study due to its properties like high latent heat value, a wide range of melting point, non-corrosive, chemically inert, and negligible volumetric change during the phase change [15]. Table 3 shows the thermophysical properties of Paraffin wax.

Table 3
Thermophysical Properties of Paraffin Wax

Sl. No.	Property	Value
1	Density, kg/m^3	748
2	Thermal conductivity, W/mK	0.26
3	Dynamic viscosity, Ns/m^2	1.856
4	Specific heat, J/kgK	2944
5	Latent heat of fusion, kJ/kg	264
6	Melting point, ◦C	48.28 - 54.21

3. Experiment Set Up and Procedure

Steady-state experiments are conducted for 30 different configurations of λ mentioned in Table 2. The low-speed wind tunnel which is used for doing experimental work. The SMPS component is always accompanied with fan for cooling purpose. As per JEDEC Solid State Technology Association (Standard No. 51-6), for electronics applications wind tunnel is used for testing the thermal performance of the IC chips under forced convection.

Initially the simulations are conducted for the natural convection where the temperature was above the threshold limit, therefore to bring down the temperature of the electronic components the two velocities (3 m/s and 5m/s) were selected which shows a considerable a drop in the temperature of the electronic components. The ambient conditions are considered to be in range of 25°C- 30°C where all the IC chips are considered at $T\infty$ at ideal conditions. With the mentioned ambient condition, a mild velocity of air must be supplied to the IC chip by using a fan to lower down the temperatures and when the IC chip is generating some amount of heat, the velocities of air can be increased gradually to keep below the safe working temperatures. IC chips are supplied with high heat flux for the maximum operating condition fetched from the data sheet provided by the manufacturer [16].

3.1 Method for Carrying out Steady-State Laminar Forced Convection Experiments

Initially, the wind tunnel maintains uniform air velocity in the test section with axial flow. This ensures a stable temperature near the ambient range (30°C) for the substrate board and IC chips. The DC power source activates, providing the required heat input to the IC chips, with precise voltage and current adjustments. The temperature logger scans through the Serial Communication Port, recording stable temperatures from each thermocouple. The temperatures of the IC, mini-channel and PCM are recorded in the computer from the data logger as explained in Figure 3.

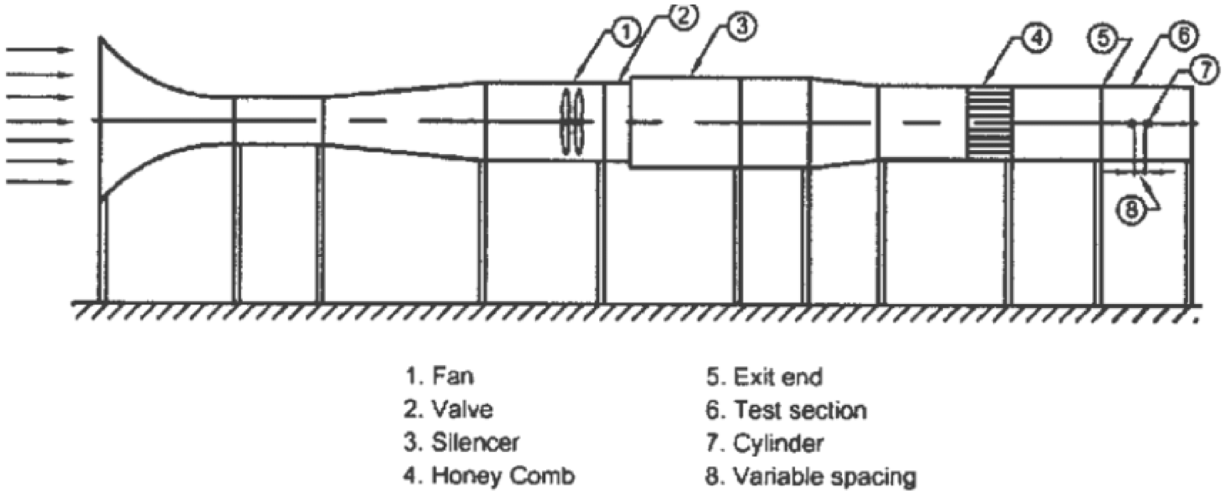

Fig. 3. Experimental Setup

3.2 Procedure for Conducting Experiment on PCM Under Natural Convection

The assembly of PCM based substrate board as shown in Figure 1 is kept in the test section for horizontal orientation. All the experiments with PCM are conducted for horizontal orientation of the substrate of the board. The ICs are supplied with volumetric heat generation (arises to different heat flux). The experiments are conducted for without PCM based substrate board and with PCM based substrate board. The temperatures of the IC, mini-channel and PCM are recorded in the computer from the data logger. The temperatures obtained from above experiments are recorded by computer and the various plots are plotted.

4. Results and Discussion

Steady-state experiments are carried out for 30 distinct configurations, as specified in Table 1, with a horizontal orientation only for with and without PCM materials substrate boards. The various temperatures were obtained. It is noted that for higher value of $\lambda = 0.19$ the temperature drop is 18.79 % with 3 m/s velocity and 26.48% with 5 m/s velocity without PCM and temperature drop is 23.58 % with 3 m/s velocity and 32.47% with 5 m/s velocity with PCM as mentioned in Figure 4, Figure 5, Figure 6 and Figure 7.

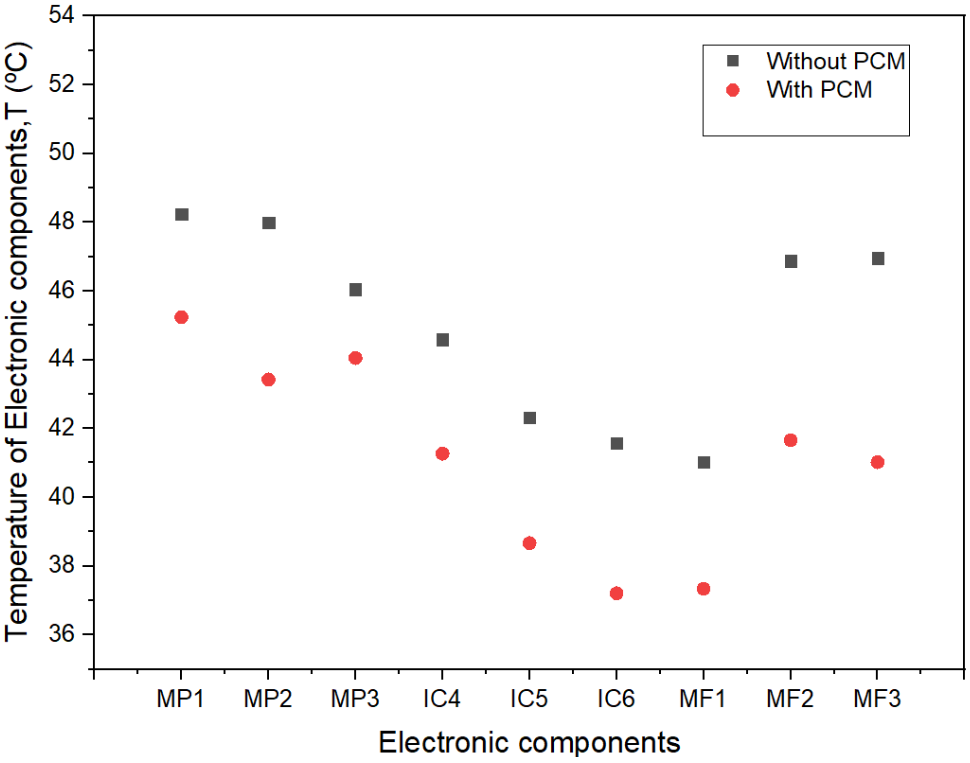

Fig. 4. Temperatures of heat sources forced convection (3 m/s) for higher lamda value 1.9

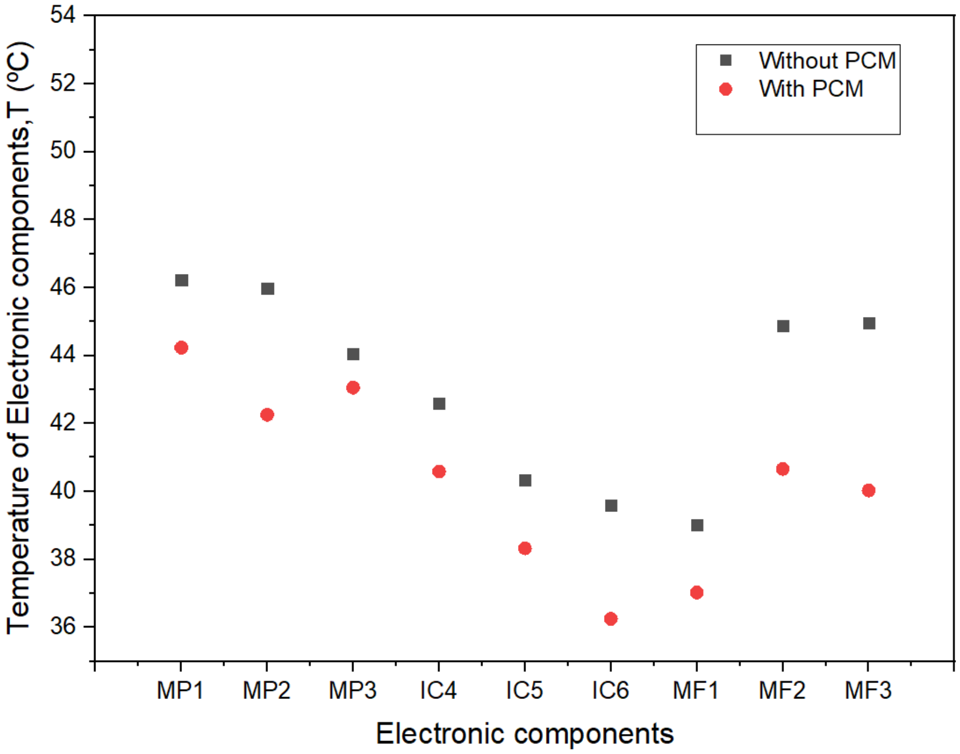

Fig. 5. Temperatures of heat sources forced convection (5 m/s) for higher lamda value 1.9

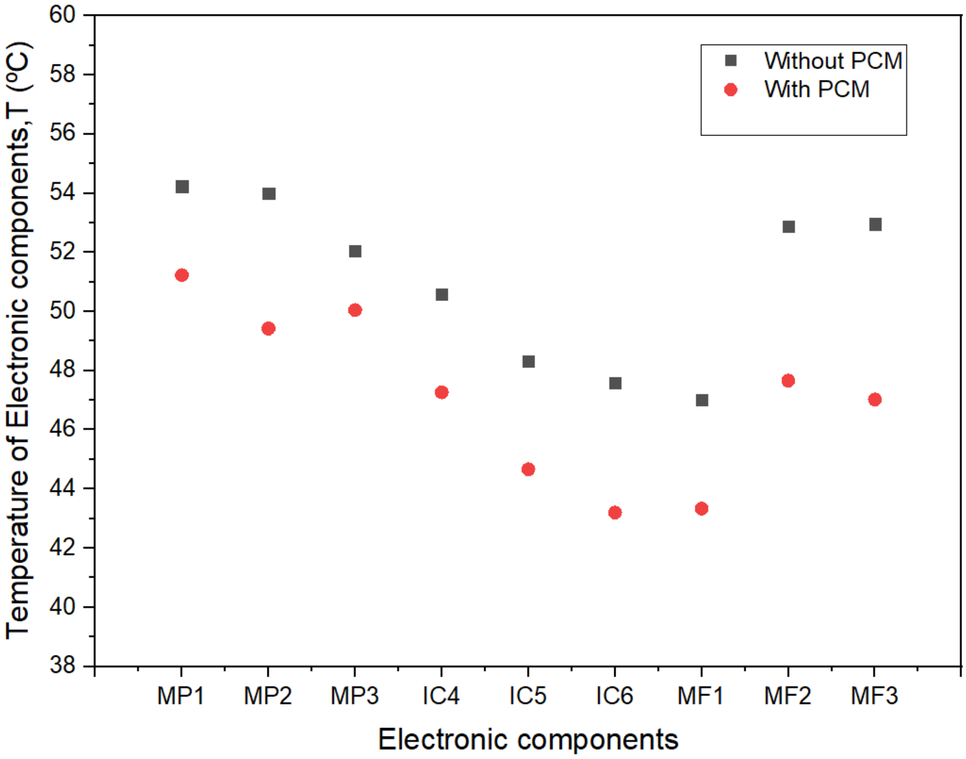

Fig. 6. Temperatures of heat sources forced convection (3 m/s) for higher lamda 0.28

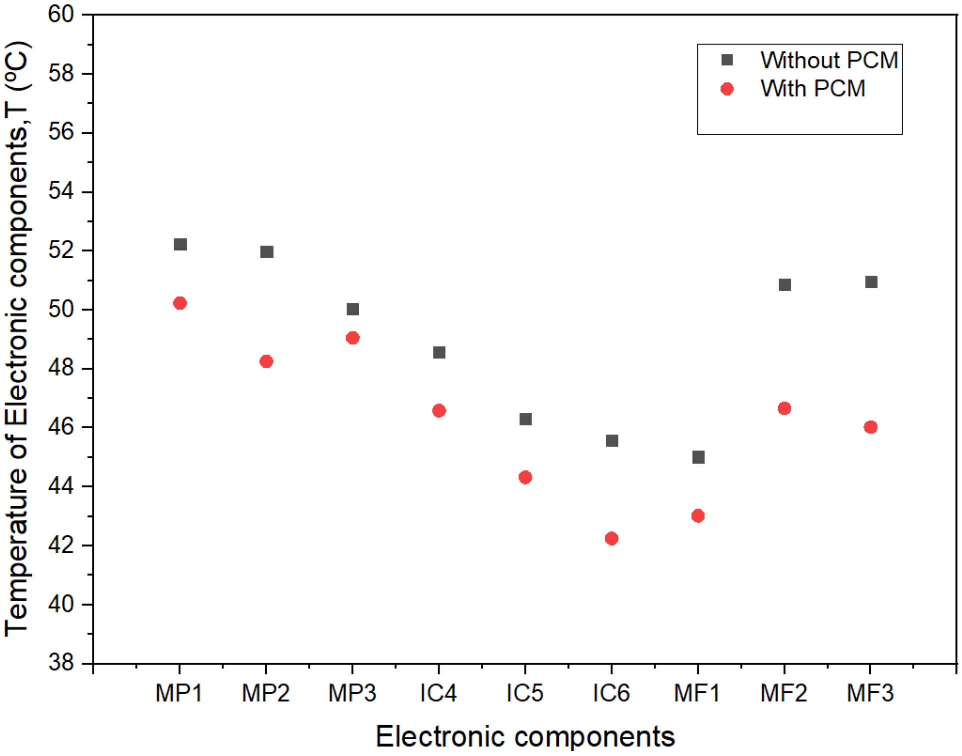

Fig. 7. Temperatures of heat sources forced convection (5 m/s) for higher lamda 0.28

The air speed is deliberately lowered to 3 m/s to examine how it influences the temperature of ECs, aiming to minimize power consumption. It is evident that employing a lower velocity leads to a temperature rise of 3.15–11.12 °C in ECs. However, this reduction in fan power consumption contributes to keeping the EC temperature below the critical threshold.

5. Conclusions

The main goal of the current chapter is to reduce further the temperature of the IC chips with the use of PCM based mini-channel under mixed convections. Steady-state experiments were conducted involving nine distinct discrete ICs positioned at various locations on a substrate board with phase-change material (PCM), while subjecting them to varying levels of heat flux. The study has yielded the following findings

i. It has been observed that the temperature strongly depends on factors such as IC size, IC positions, and heat flux supplied to the ICs. Additionally, the non-dimensional geometric distance parameter, λ, is influenced significantly by both size and position.
ii. It is noted that for higher value of $\lambda = 0.19$ the temperature drop is 18.79 % with 3 m/s velocity and 26.48% with 5 m/s velocity without PCM and temperature drop is 23.58 % with 3 m/s velocity and 32.47% with 5 m/s velocity with PCM.
iii. As per the results of decreased the temperature of IC chips with use of PCM, the life of chips also increases and need to operate within optimal temperature range.

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